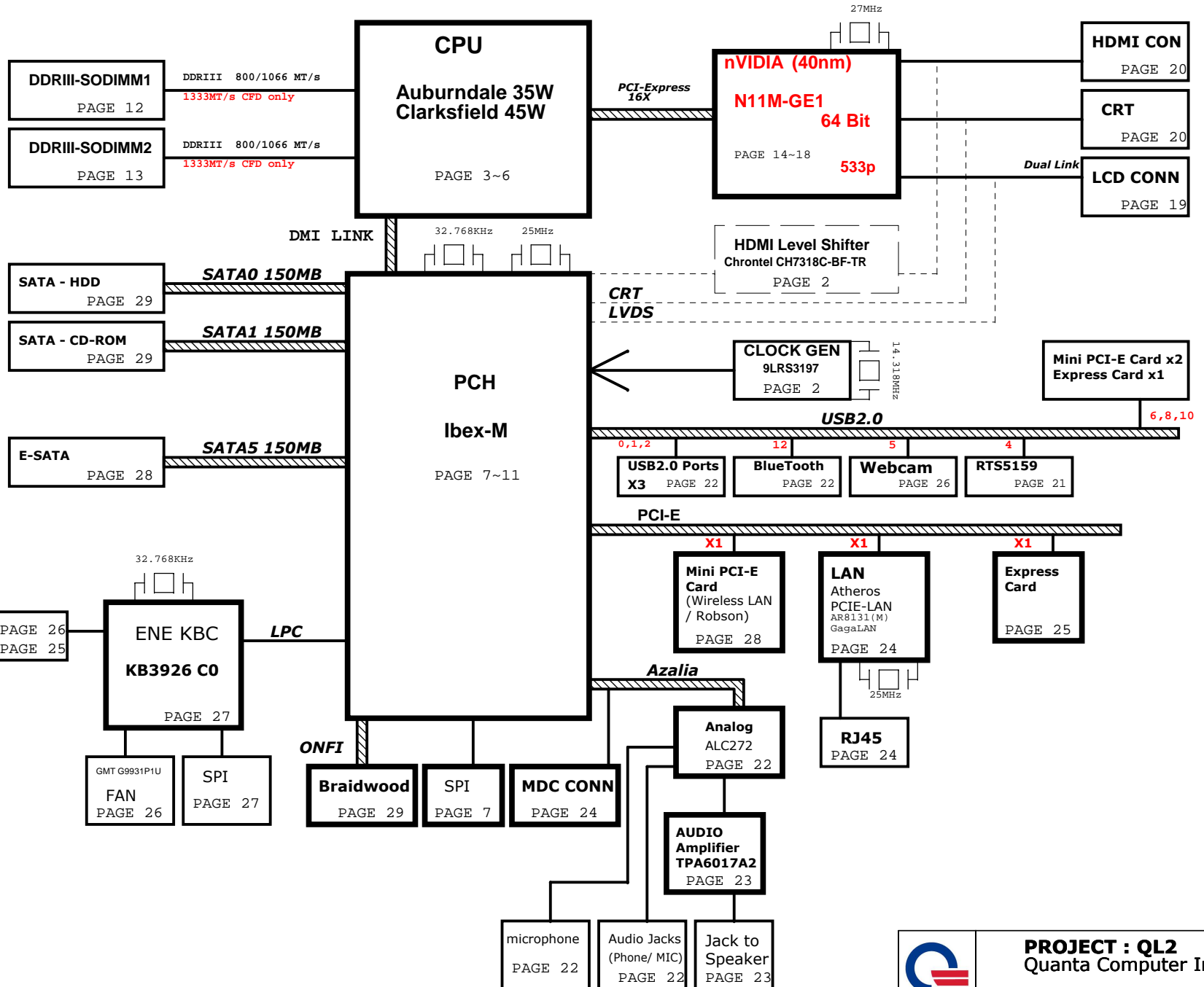
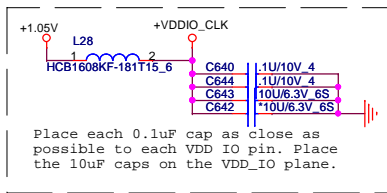


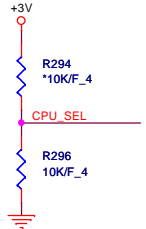
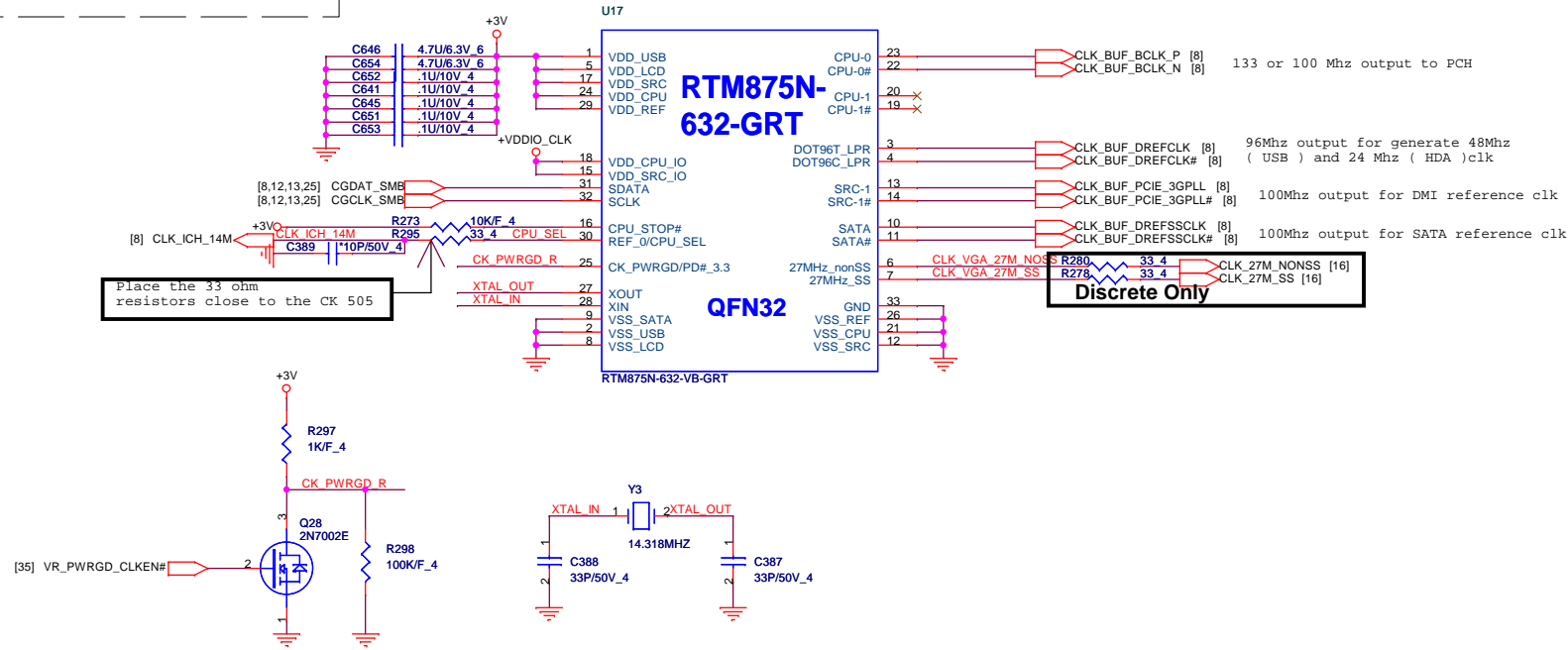
QL2 (14W) BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT





CLOCK GENERATOR



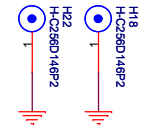
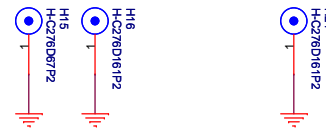
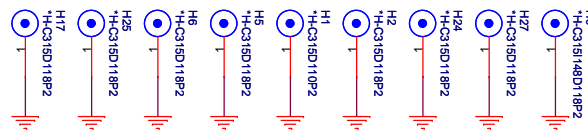
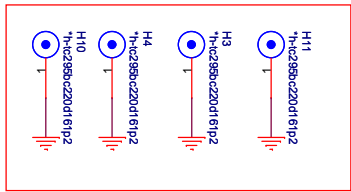
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.

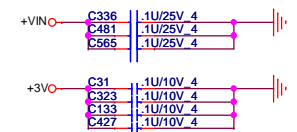
PAD and HOLE

MINI CARD Hole.

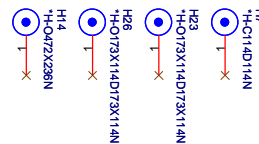
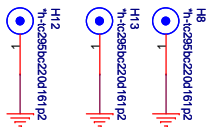
MDC Hole.



EMI capacitive

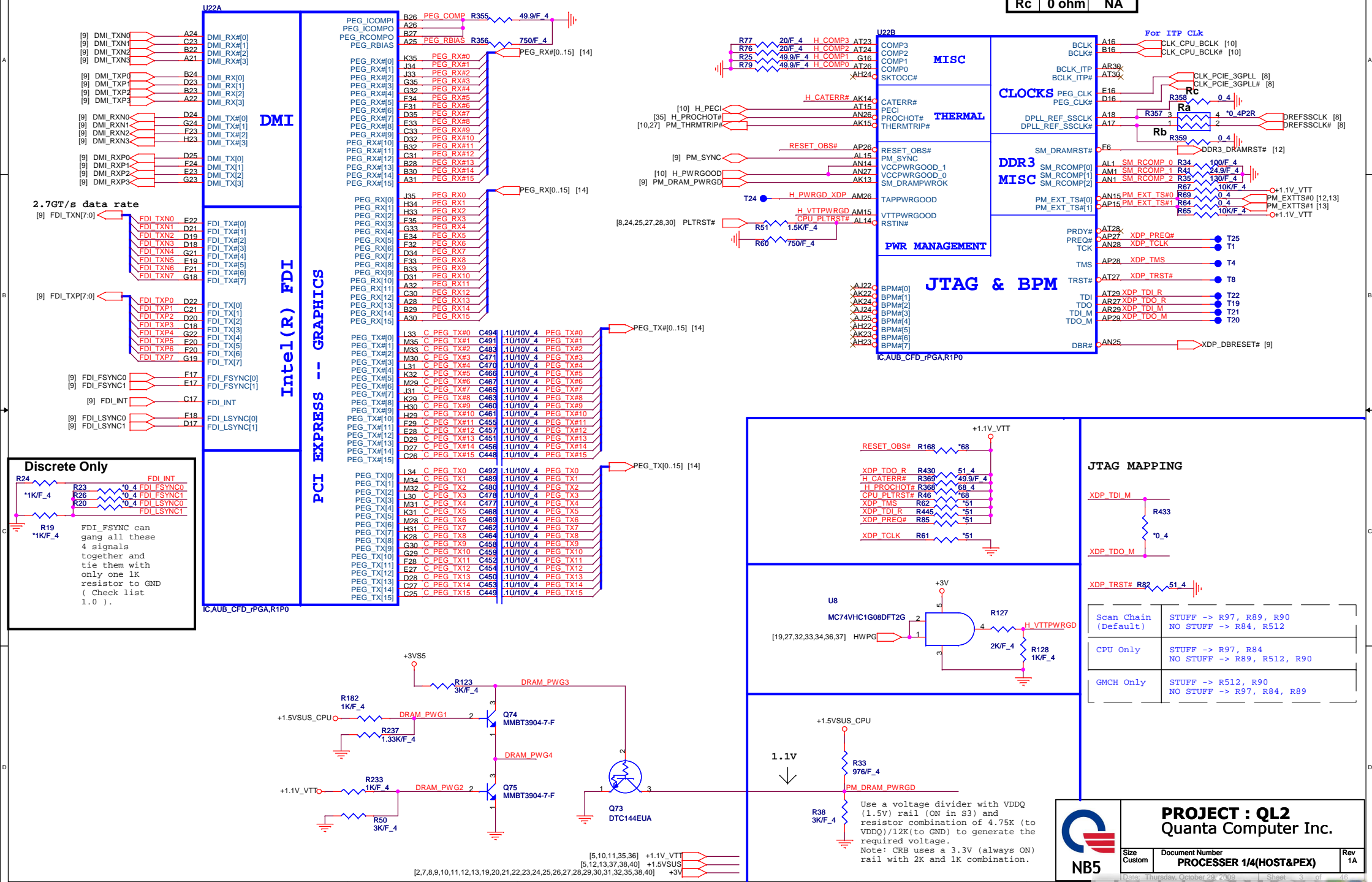


VGA bracket Hole.

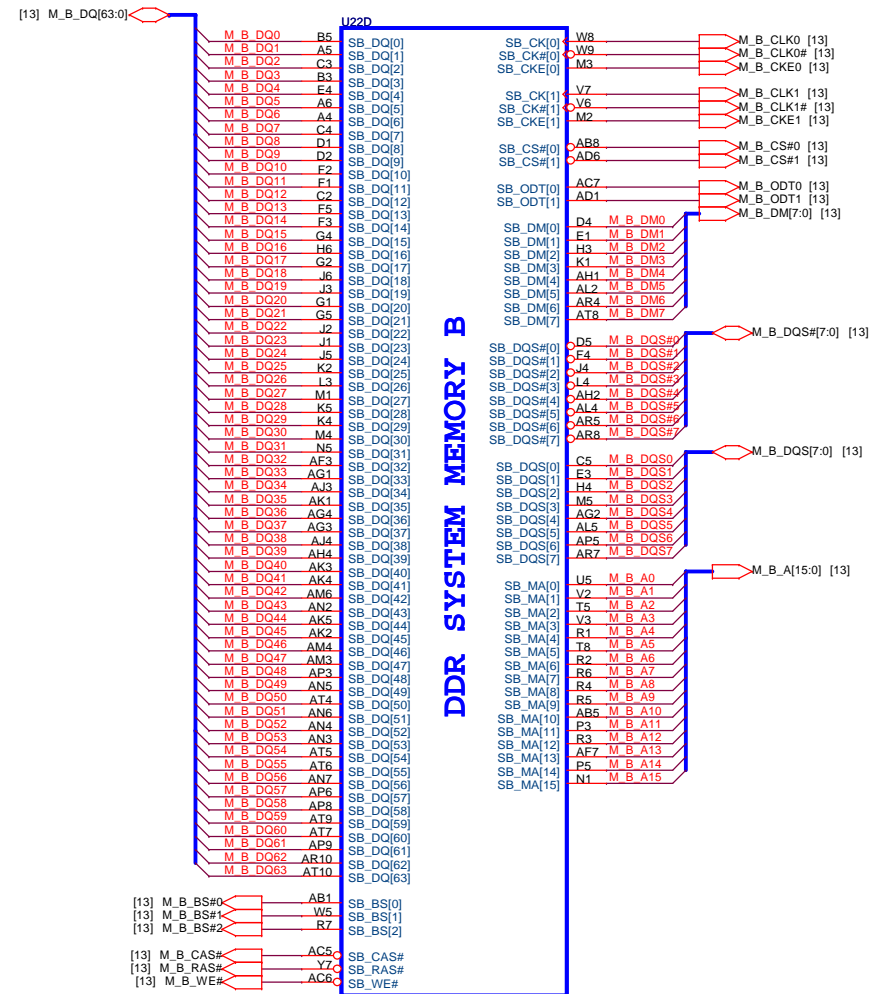
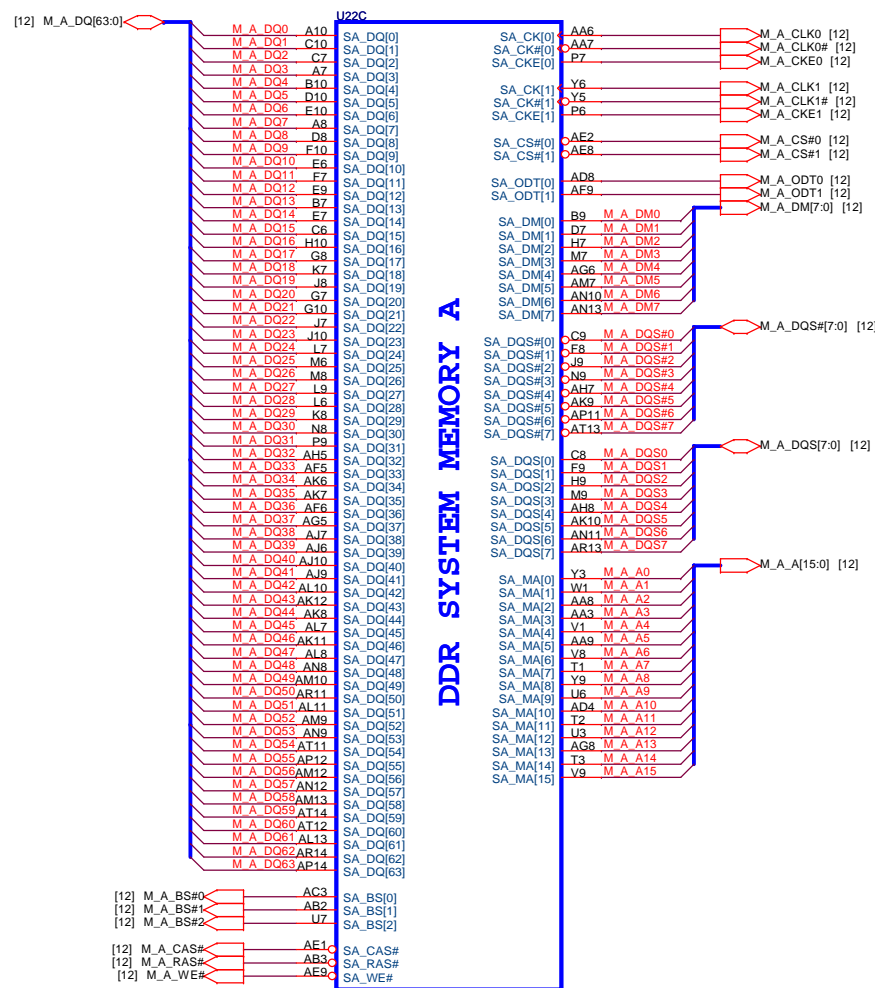


	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

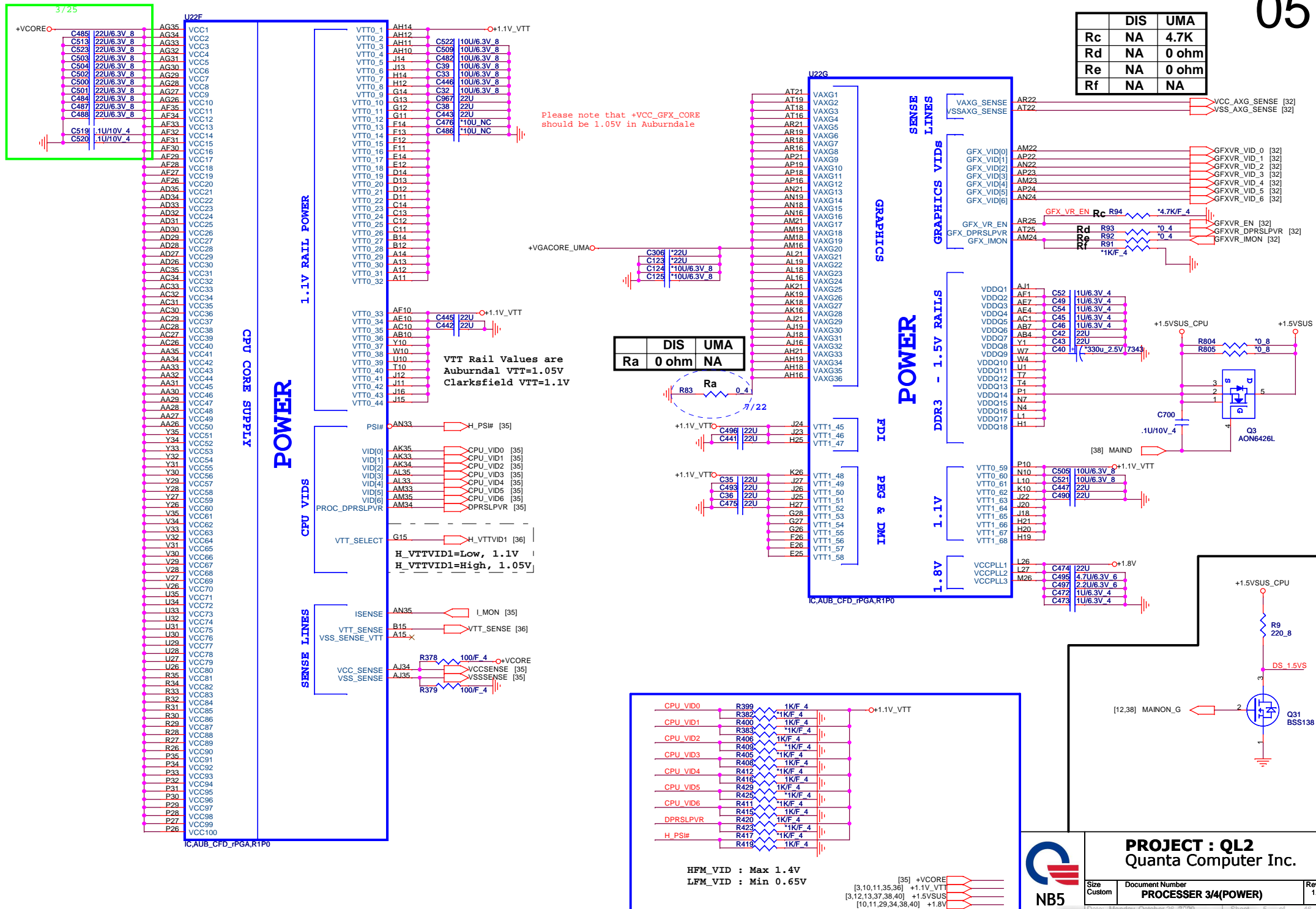
03



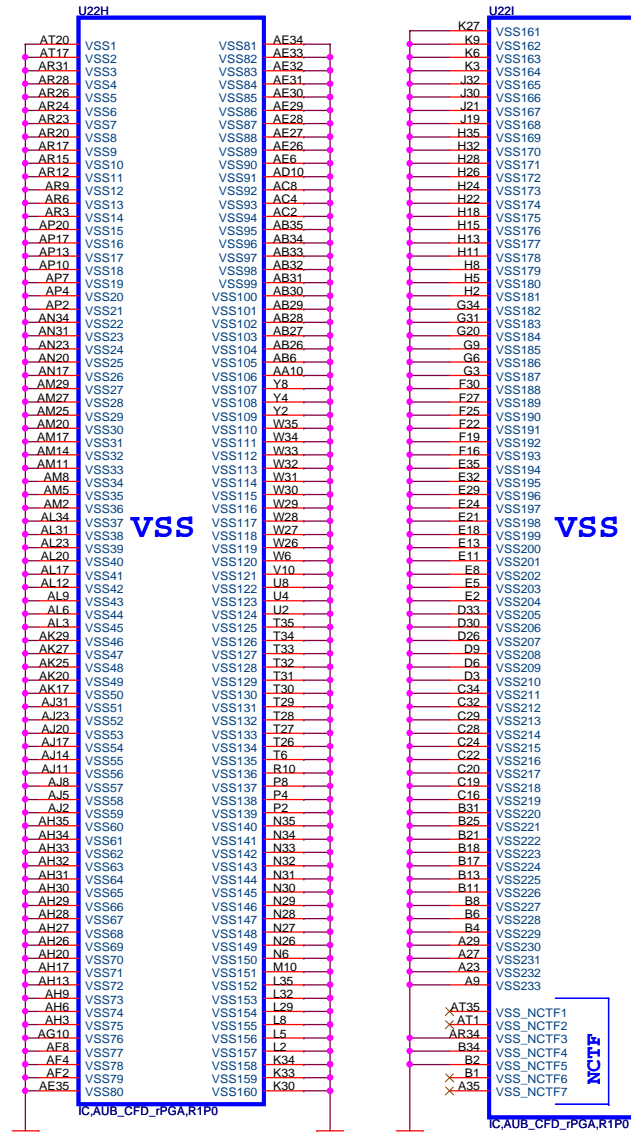
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

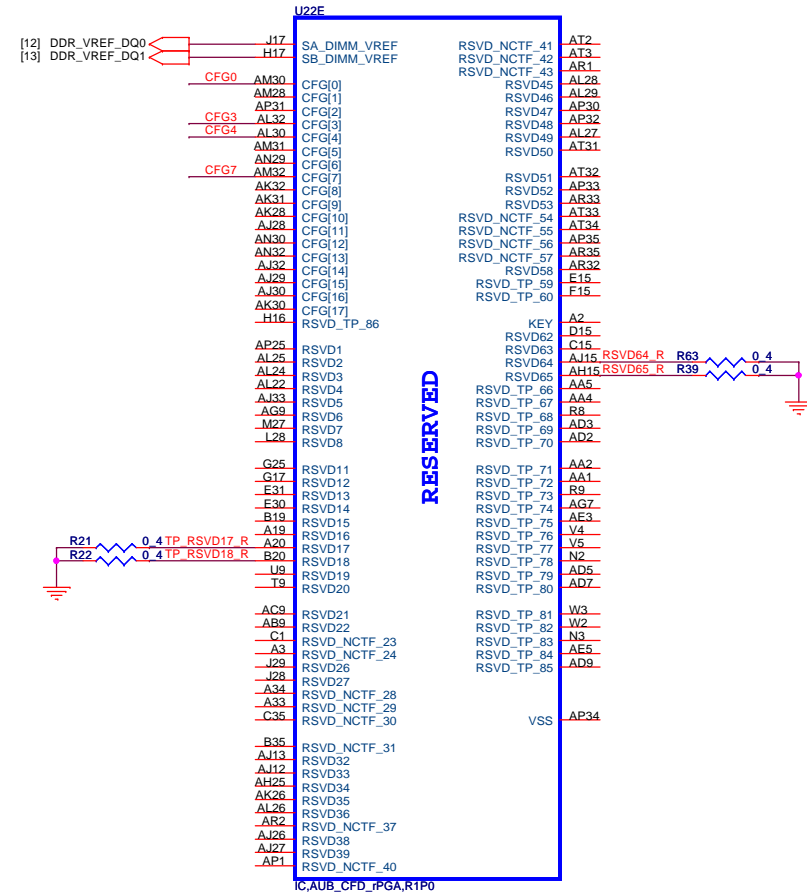


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01k \pm 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

For discrete only

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```

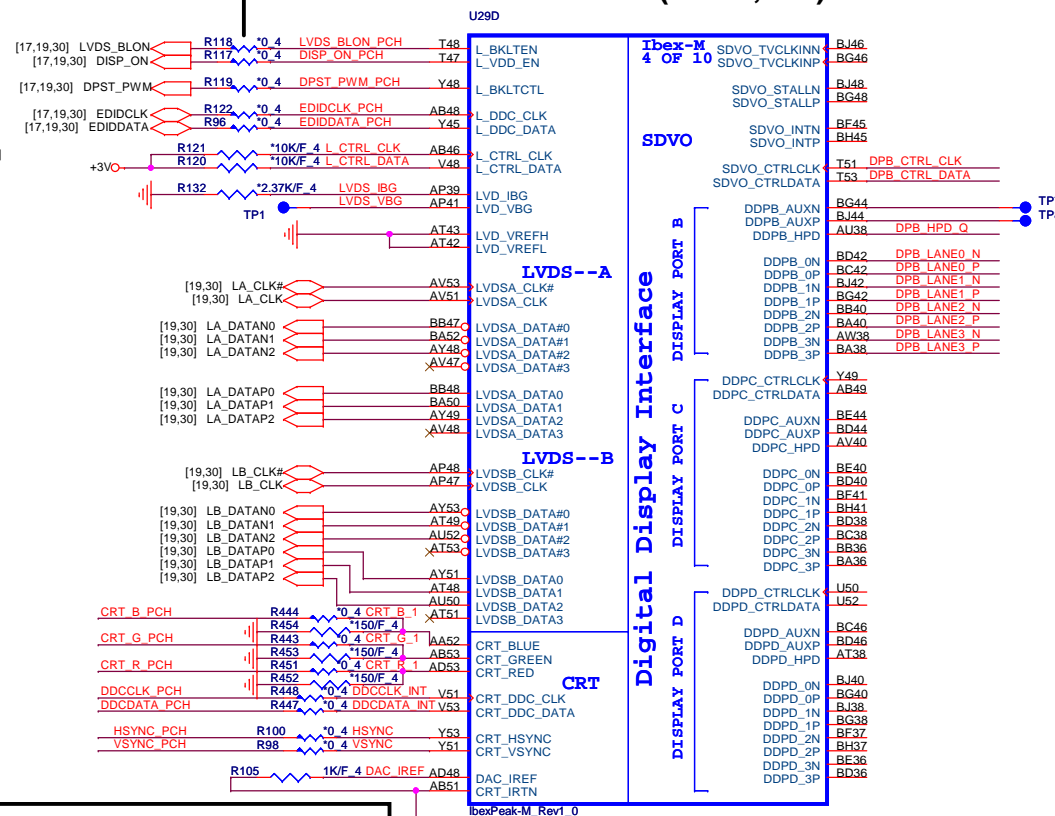
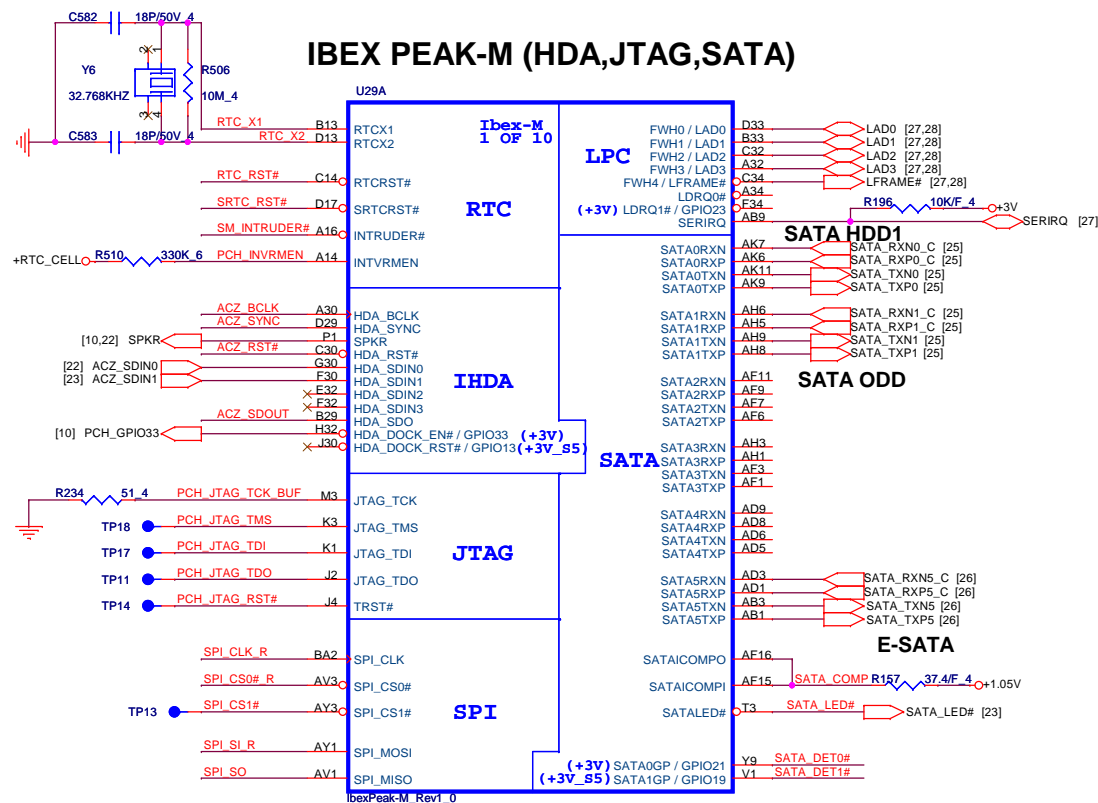


PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number PROCESSER 4/4(GND)	Rev 1A
Date: Monday, October 26, 2009		Sheet 6 of 46

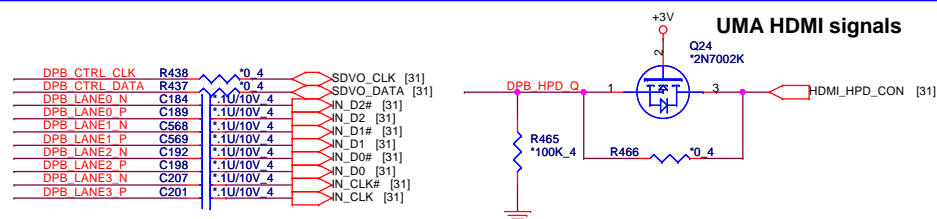
UMA LVDS & CRT signals

IBEX PEAK-M (LVDS,DDI)

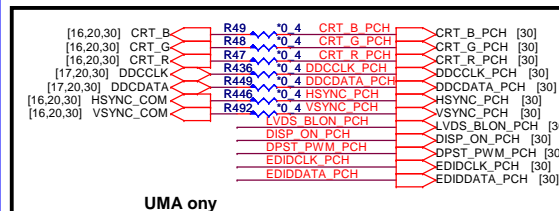


1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

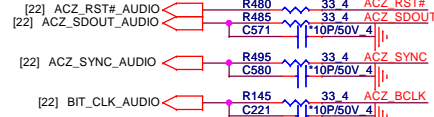
UMA HDMI signals



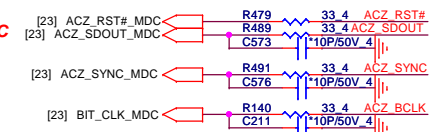
UMA only



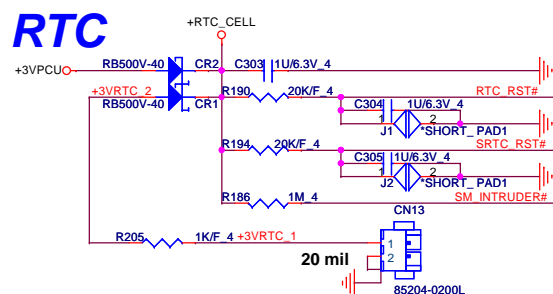
For AUDIO



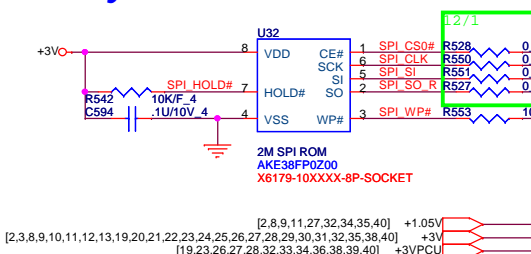
For MDC



RTC



2M byte SPI ROM for ME



2M byte SPI ROM for ME

MXIC: AKE38FP0Z00
WINBOND: AKE38FP0N01
AIT: AKE38ZN0800

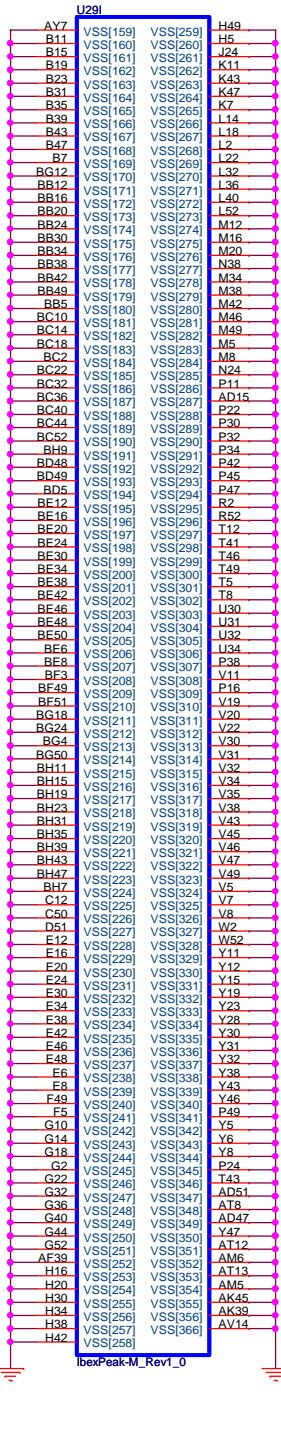
SPI ROM Socket

DG008000031

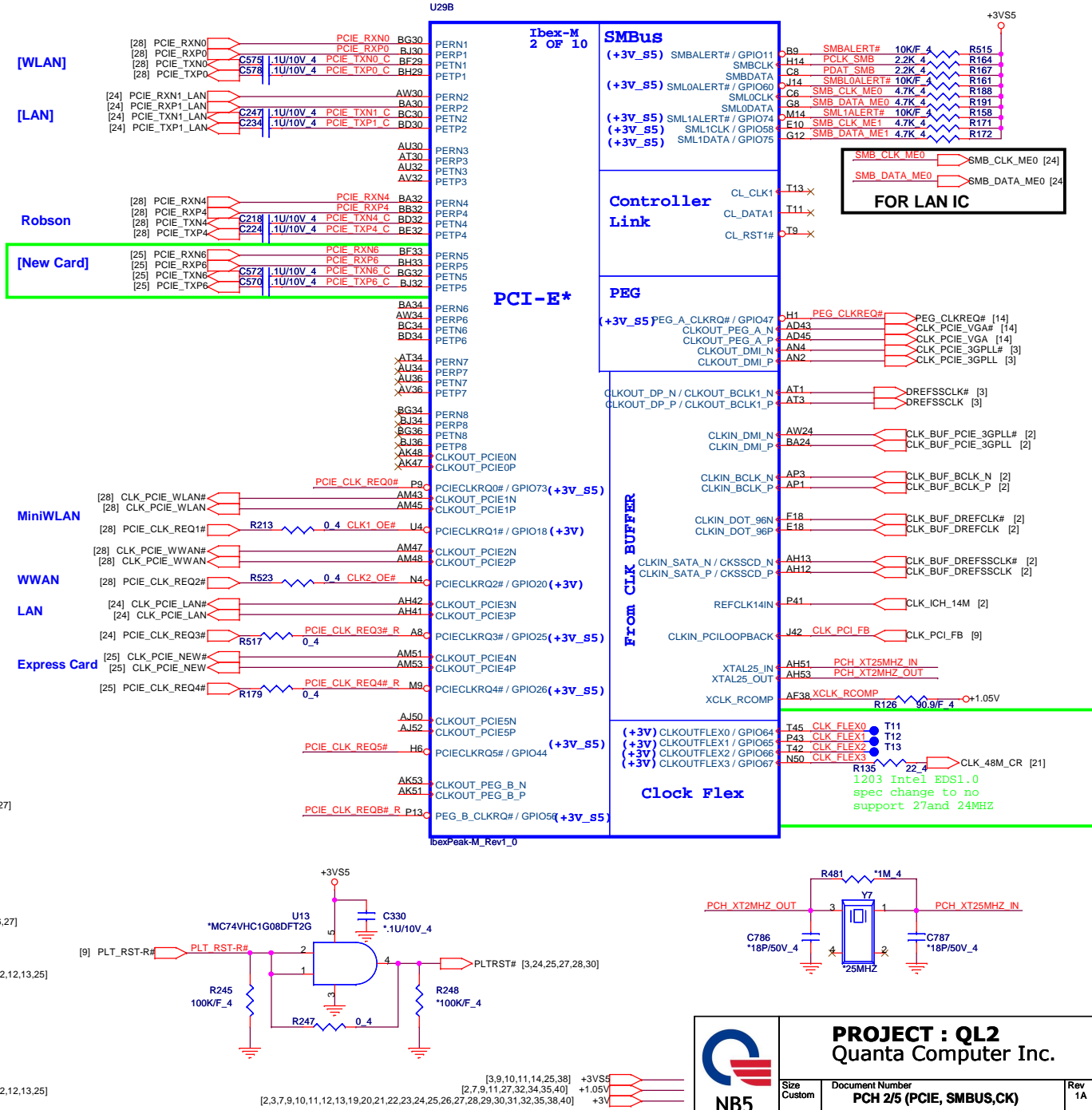


PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number PCH 1/5 (SATA,HDA,LPC)	Rev 1A
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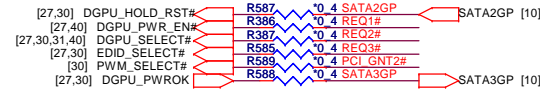


IBEX PEAK-M (PCI-E, SMBUS, CLK)



IBEX PEAK-M (PCI,USB,NVRAM)

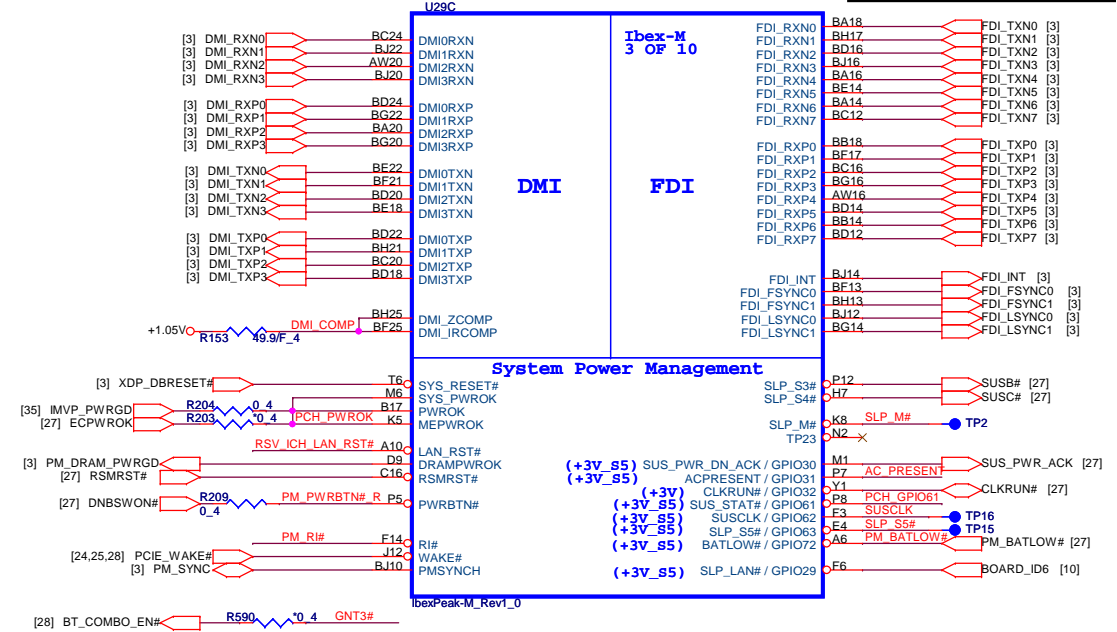
For Switchable only



Discrete Only



IBEX PEAK-M (DMI,FDI,GPIO)



USB

ESATA-USB

Card reader

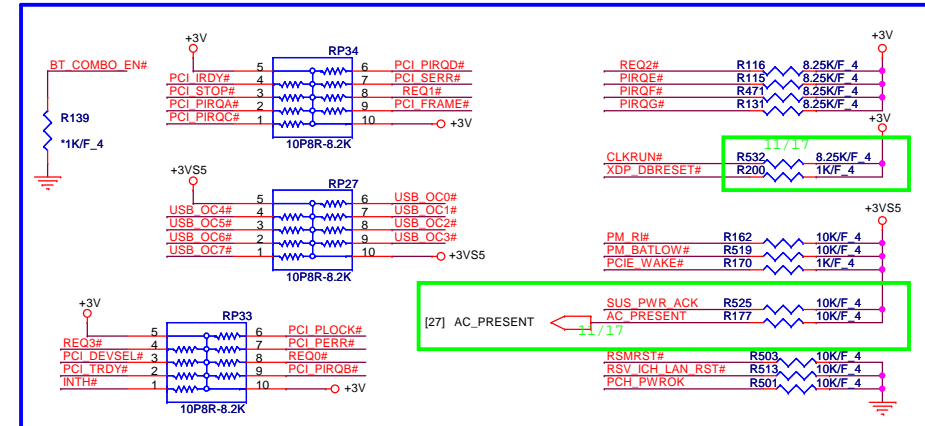
Camera

NEWCARD

WLAN

WWAN

Blue tooth



PROJECT : QL2
Quanta Computer Inc.

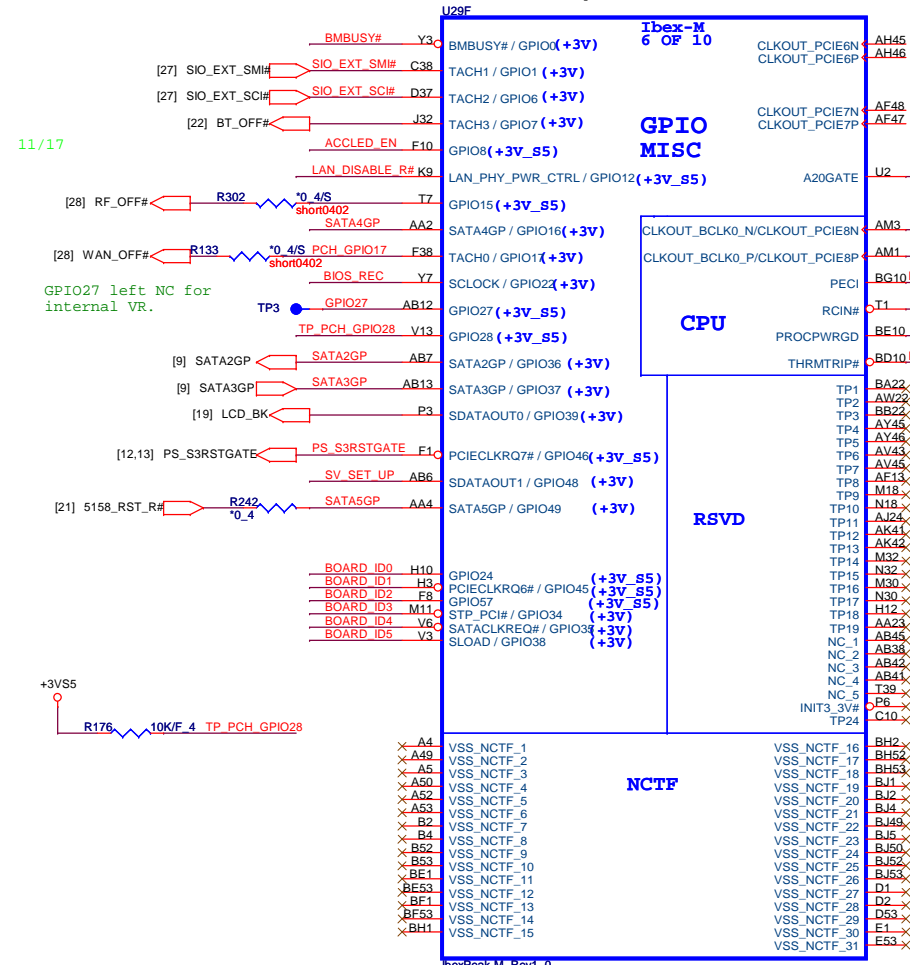
Size	Document Number	Rev
Custom	PCH 3/5(PCI,ONFI,USB,DMI)	1A

Date: Monday, October 26, 2009 Sheet 9 of 46

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

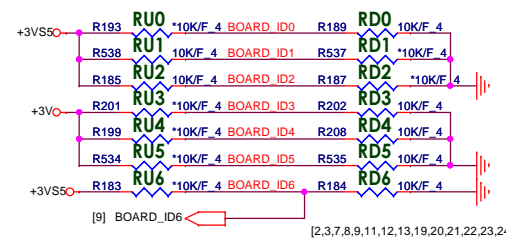
10



Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6" / 14"			0=QL4/TW9 1=QL2/SW9				
MDC				0=YES 1=NO			
Braidwood					0=YES 1=NO		

BOARD ID SETTING

Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)



Al6 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = Al6 swap override/Top-Block Swap Override enabled
High = Default

SV SET UP R198

SV_SET_UP

1-X High = Strong (Default)

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

NV_ALE

High = Enable
Low = Disable

DMI Termination Voltage

NV_CLE

Set to Vcc when LOW
Set to Vcc/2 when HIGH

No Reboot Strap

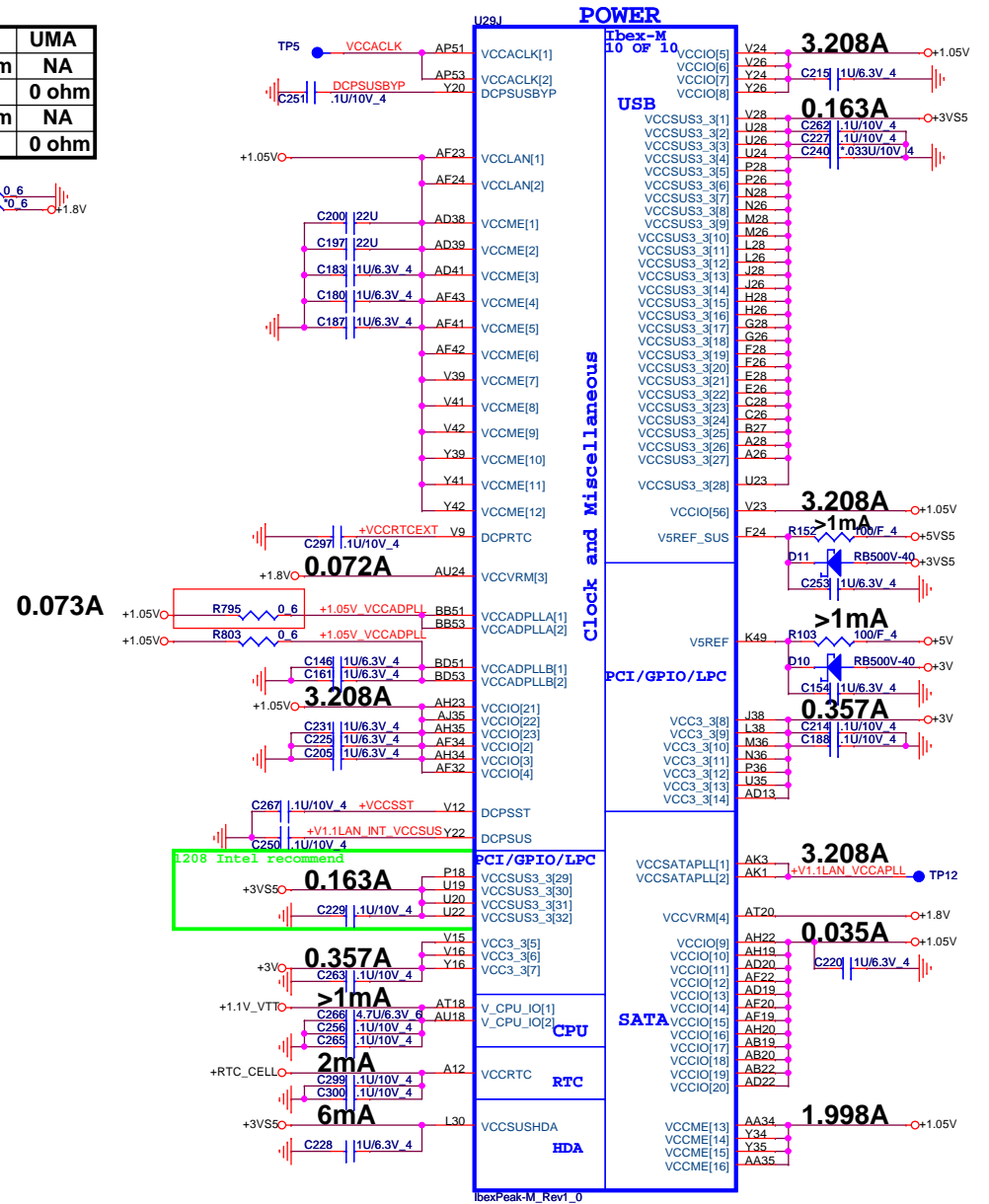
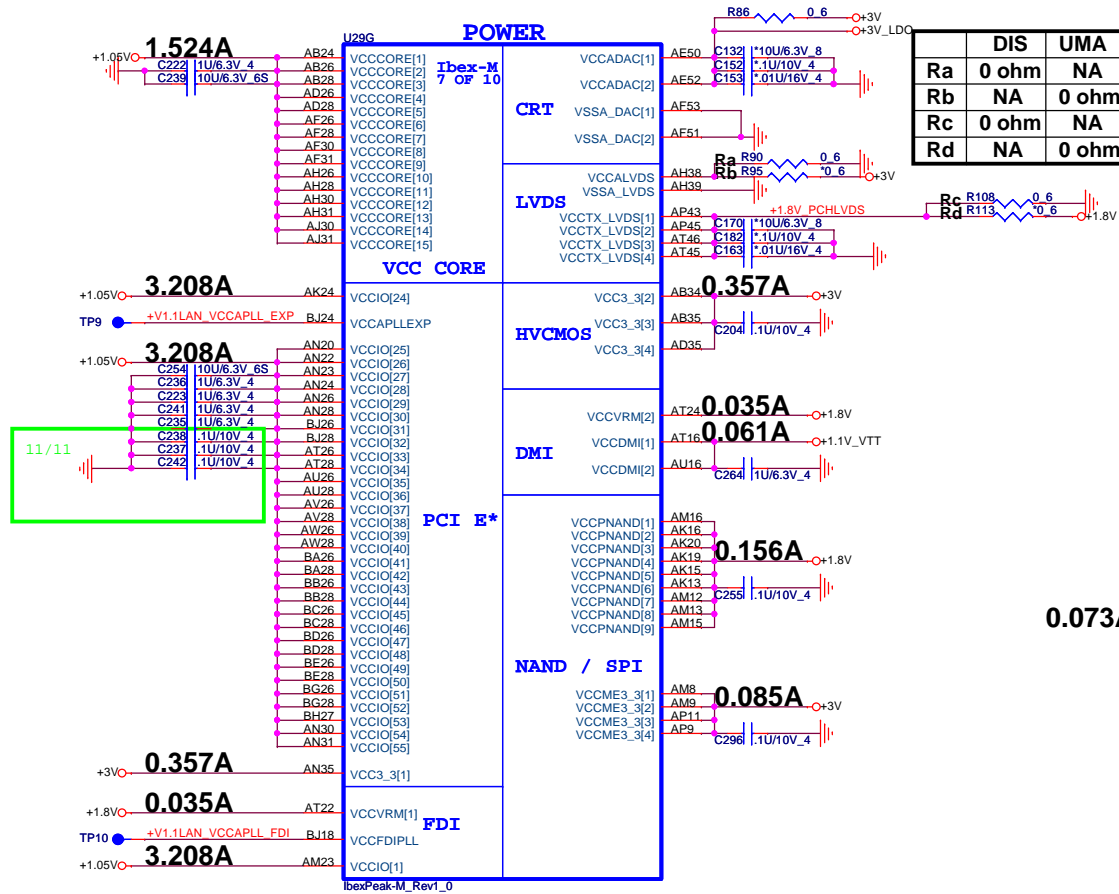
SPKR

PCH_GPIO33

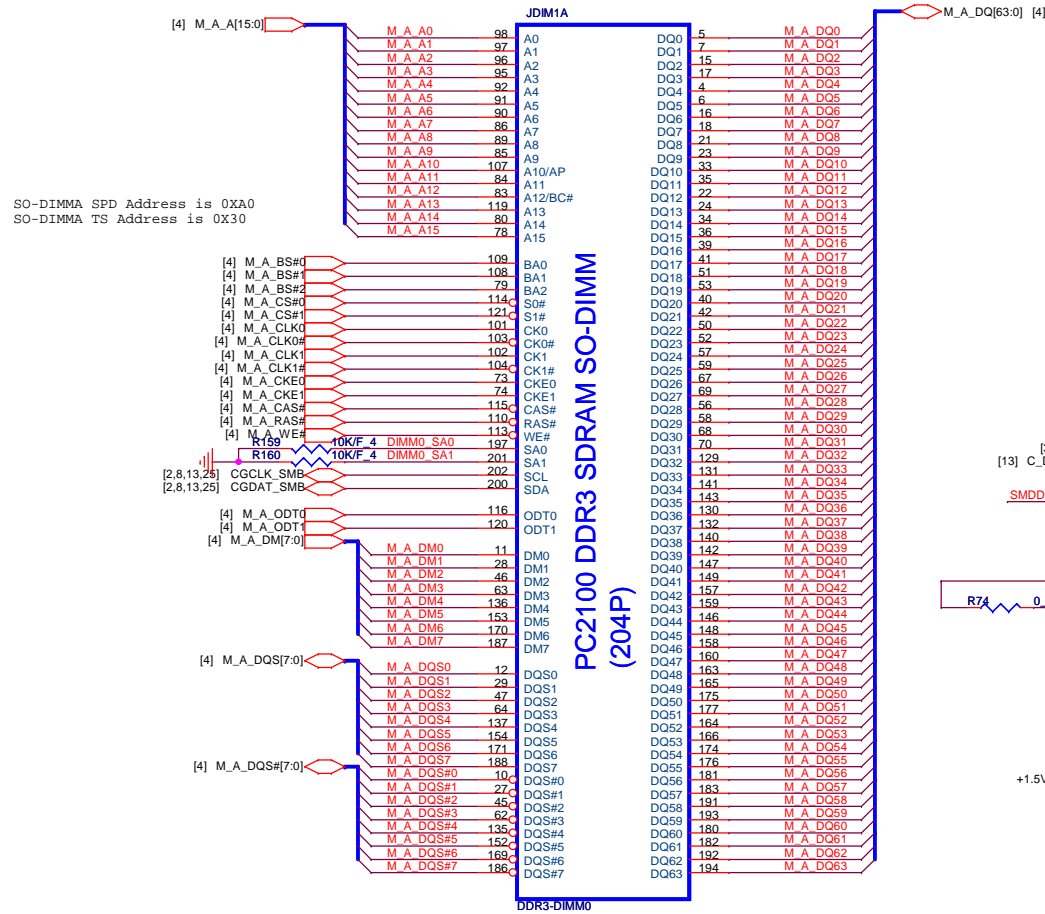
PROJECT : QL2
Quanta Computer Inc.

Size Custom Document Number **PCH 4/5 (GPIO & Strap)** Rev 1A

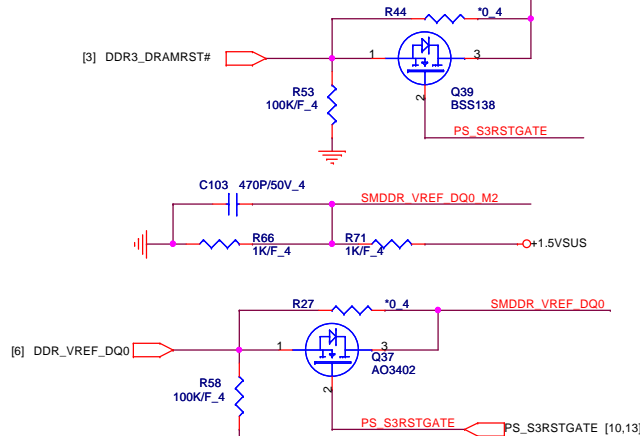
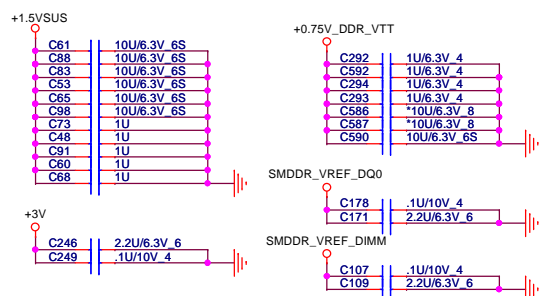
Date: Monday, October 26, 2009 Sheet 10 of 46



[2,7,8,9,27,32,34,35,40] +1.05V
 [3,5,10,35,36] +1.1V_VTT
 [5,10,29,34,38,40] +1.8V
 [2,3,7,8,9,10,12,13,19,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
 [3,8,9,10,14,25,38] +3VS5
 [20,22,23,25,26,28,30,31,38] +5V
 [38] +5VS5



Place these Caps near So-Dimm0.

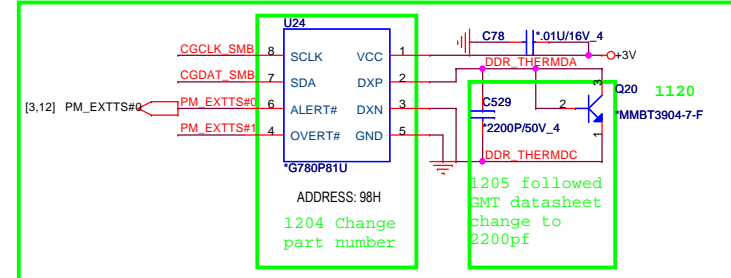
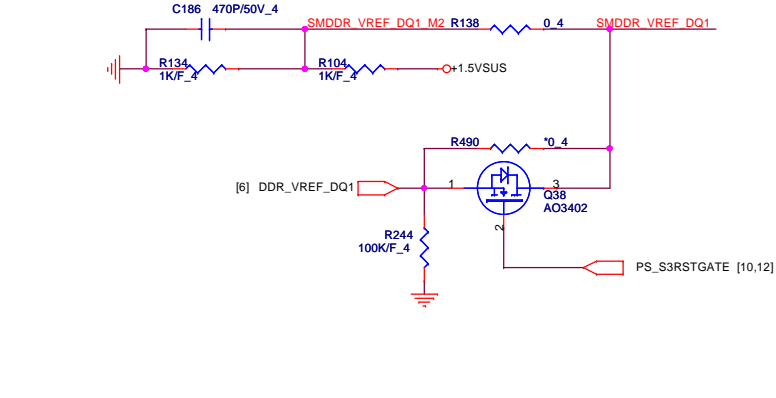
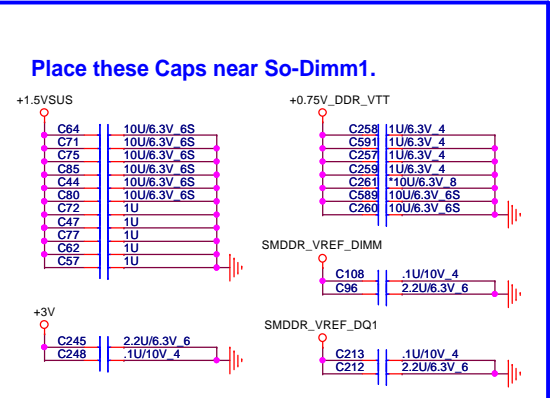
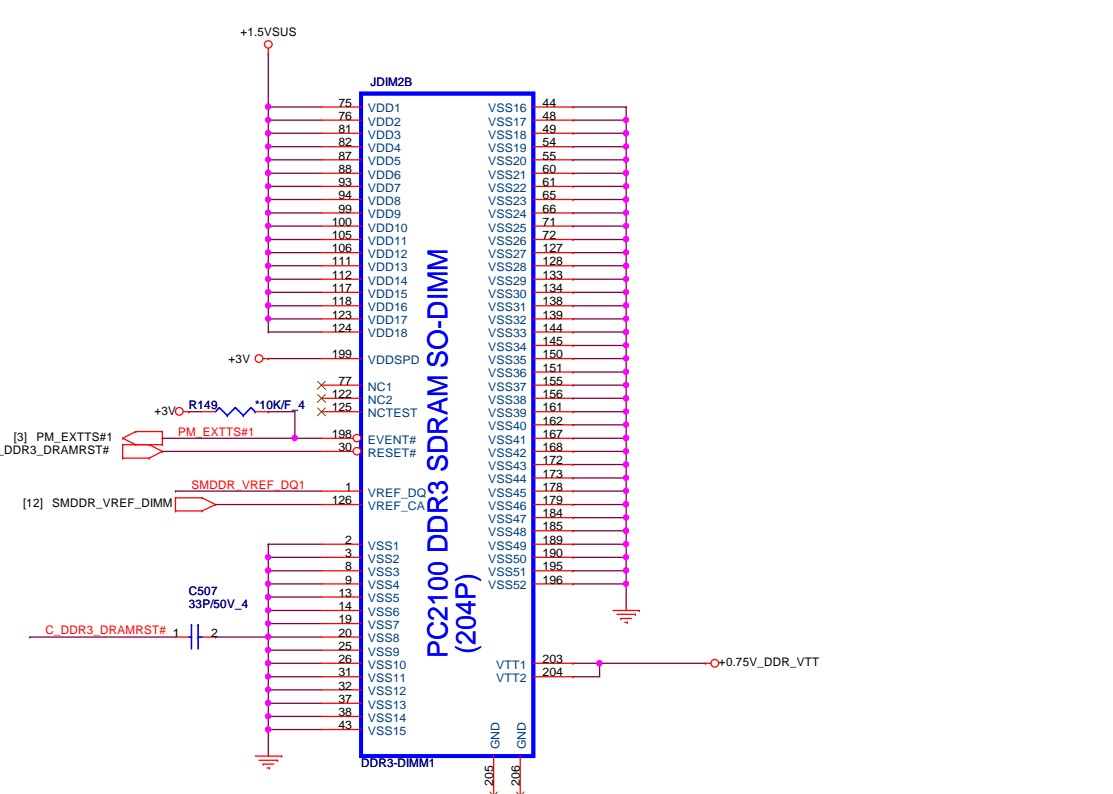
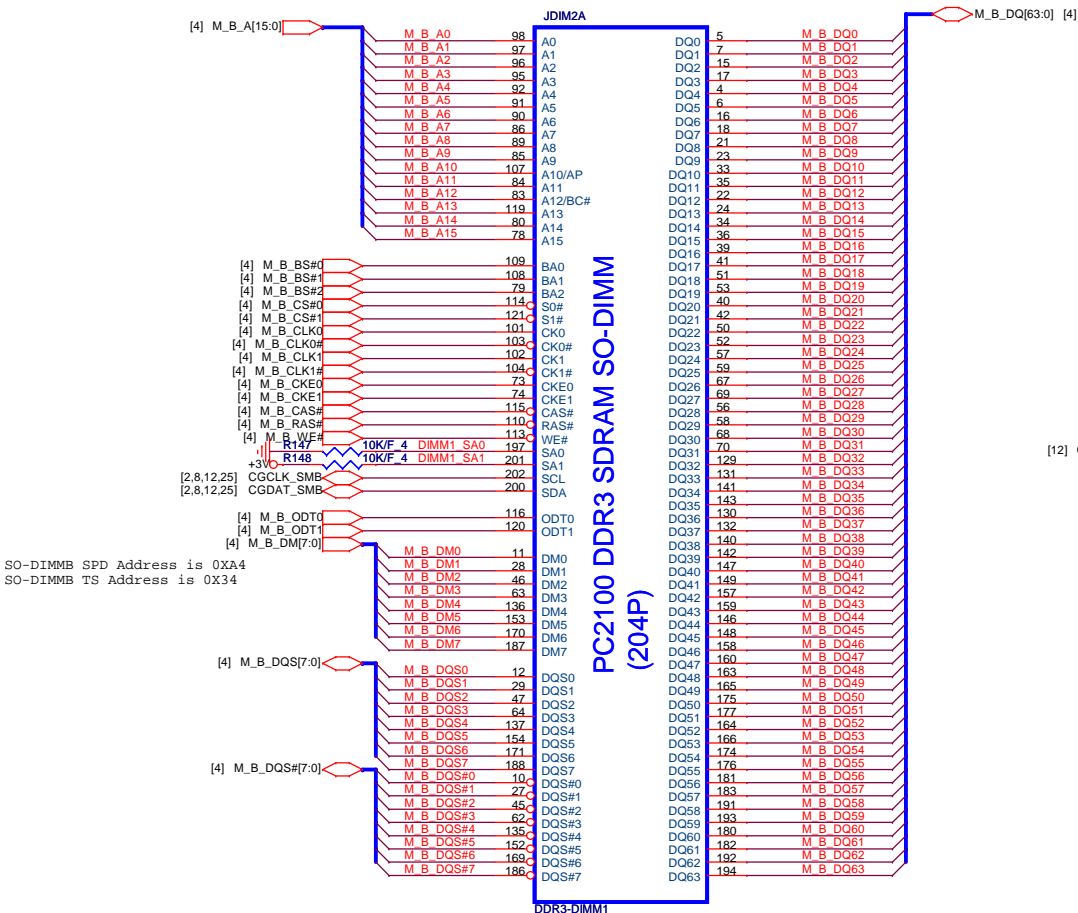


[13,37] +0.75V_DDR_VTT
[3,5,13,37,38,40] +1.5VSUS
[7,19,23,26,27,28,32,33,34,36,38,39,40] +3V
[27,32,33,34,35,36,37,38] +5VPCU

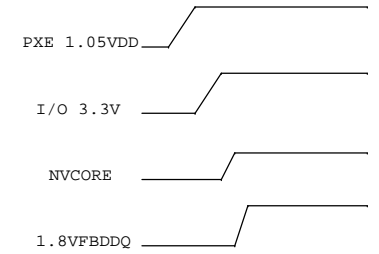


PROJECT : QL2
Quanta Computer Inc.

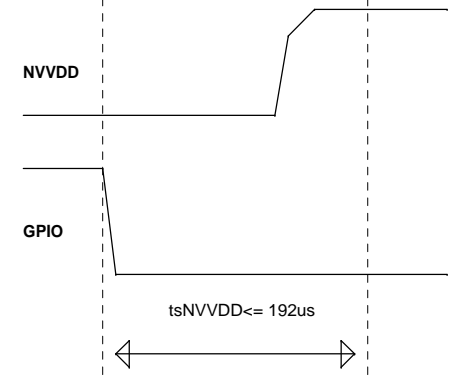
Size Custom	Document Number DDR3 DIMM-0	Rev 1A
Date: Monday, October 26, 2009	Sheet 12 of 46	



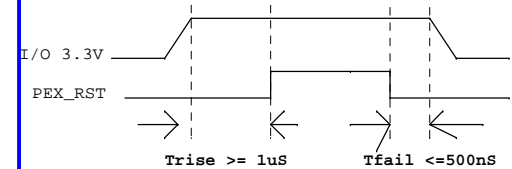
power up sequence



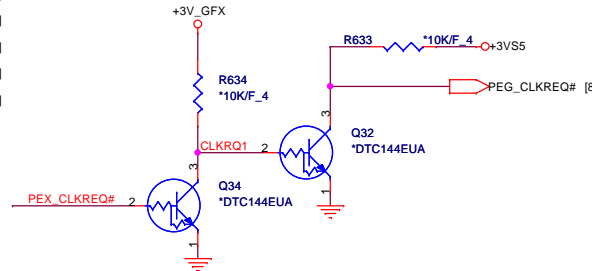
NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



For Switchable only

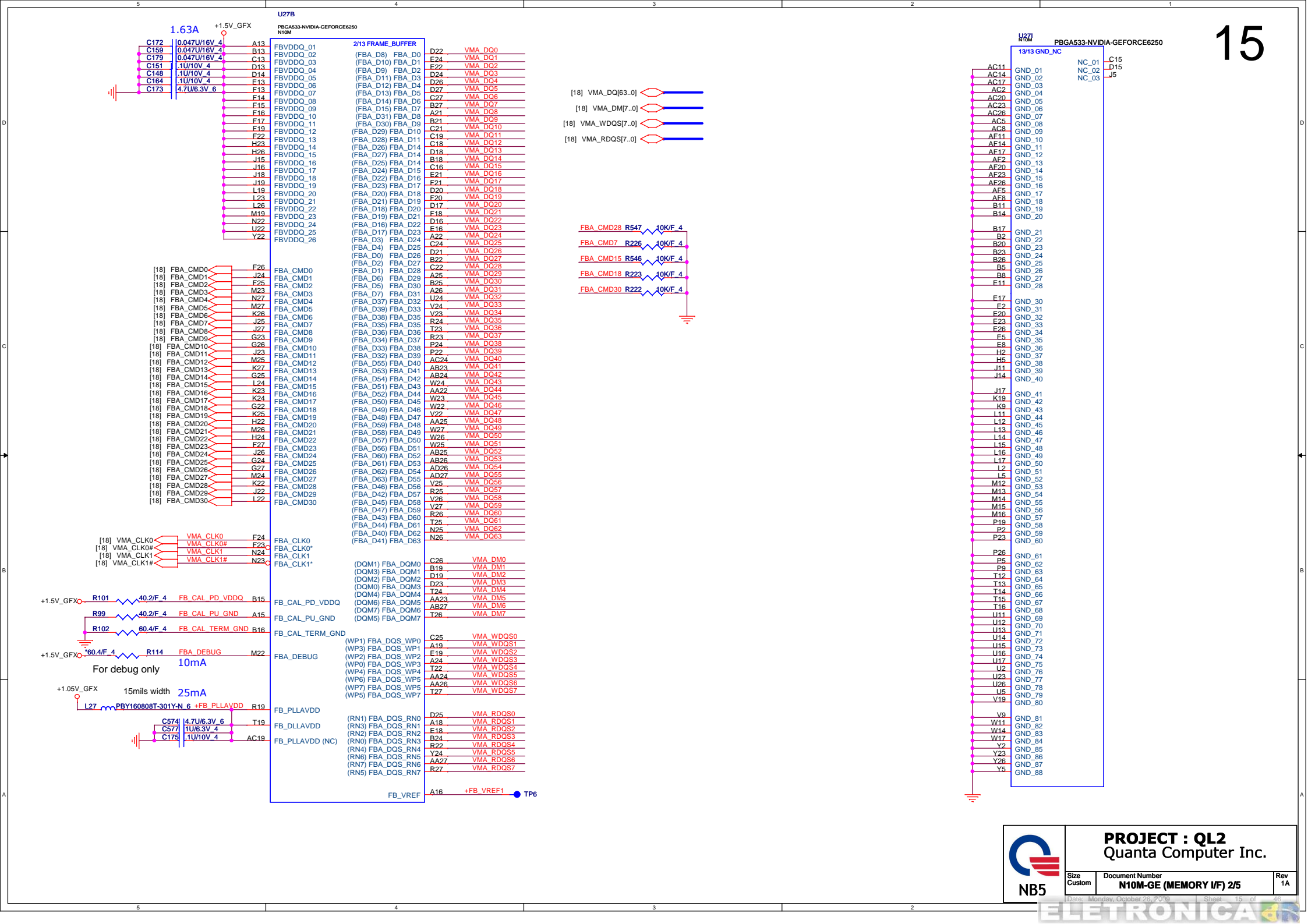


VGA Thermal Circuit => Del 6/16



PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NB5-GE (PCIE V/F) 1/5	1A
Date: Monday, October 26, 2009	Sheet 14 of 46	



CRT_R DGPU	R473	0 4	CRT_R	CRT_R	[7,20,30]
CRT_G DGPU	R474	0 4	CRT_G	CRT_G	[7,20,30]
CRT_B DGPU	R475	0 4	CRT_B	CRT_B	[7,20,30]
HSYNC DGPU	R476	0 4	HSYNC_COM	HSYNC_COM	[7,20,30]
VSYNC DGPU	R477	0 4	VSYNC_COM	VSYNC_COM	[7,20,30]

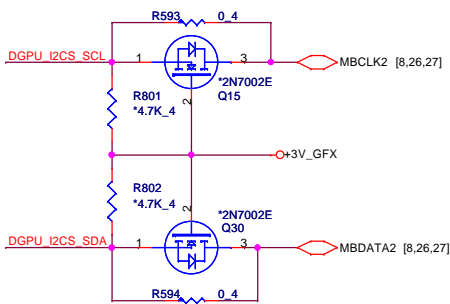
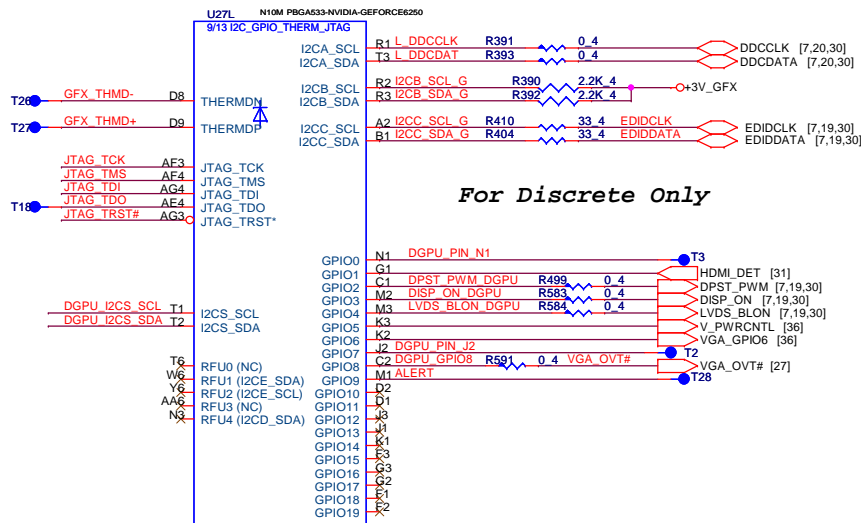
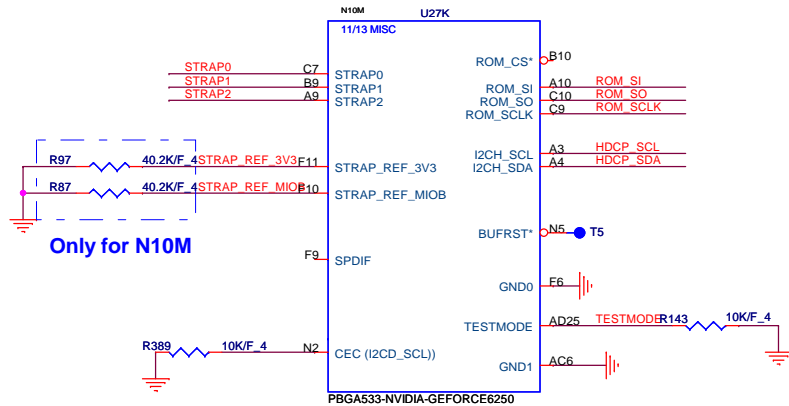
Close to GPU

SPREAD SPECTRUM == >Del 6/16

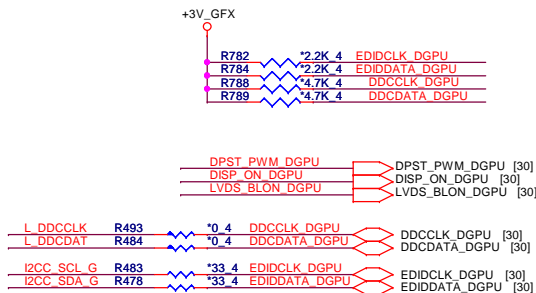


PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number N10M-GE (DISPLAY) 3/5	Rev 1A
Date: Wednesday, October 28, 2009		Sheet 16 of 46



Mount Q15, Q30, R801, R802
For Switchable only



For Switchable only

CHIP	PCI_DEVID:	STRAP2
N11P-GE1	0x0A29	1001 PU 10K
N11M-GE1	0x0A75	1010 PD 30K

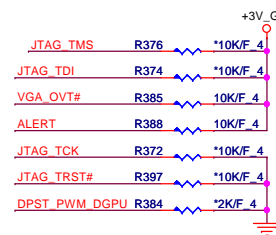
Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)] Default: Hynix VRAM
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
 30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
 35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

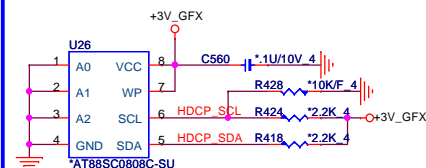
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	K4W1G1646E-EC12	PD 20K
0101		Reserved		
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	



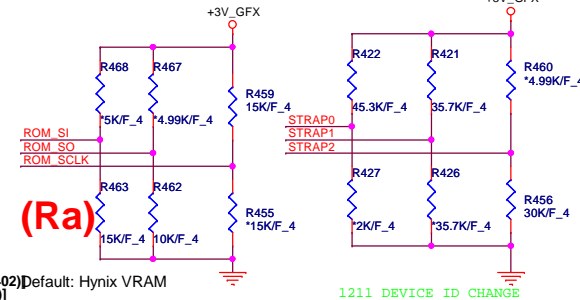
HDCP ROM



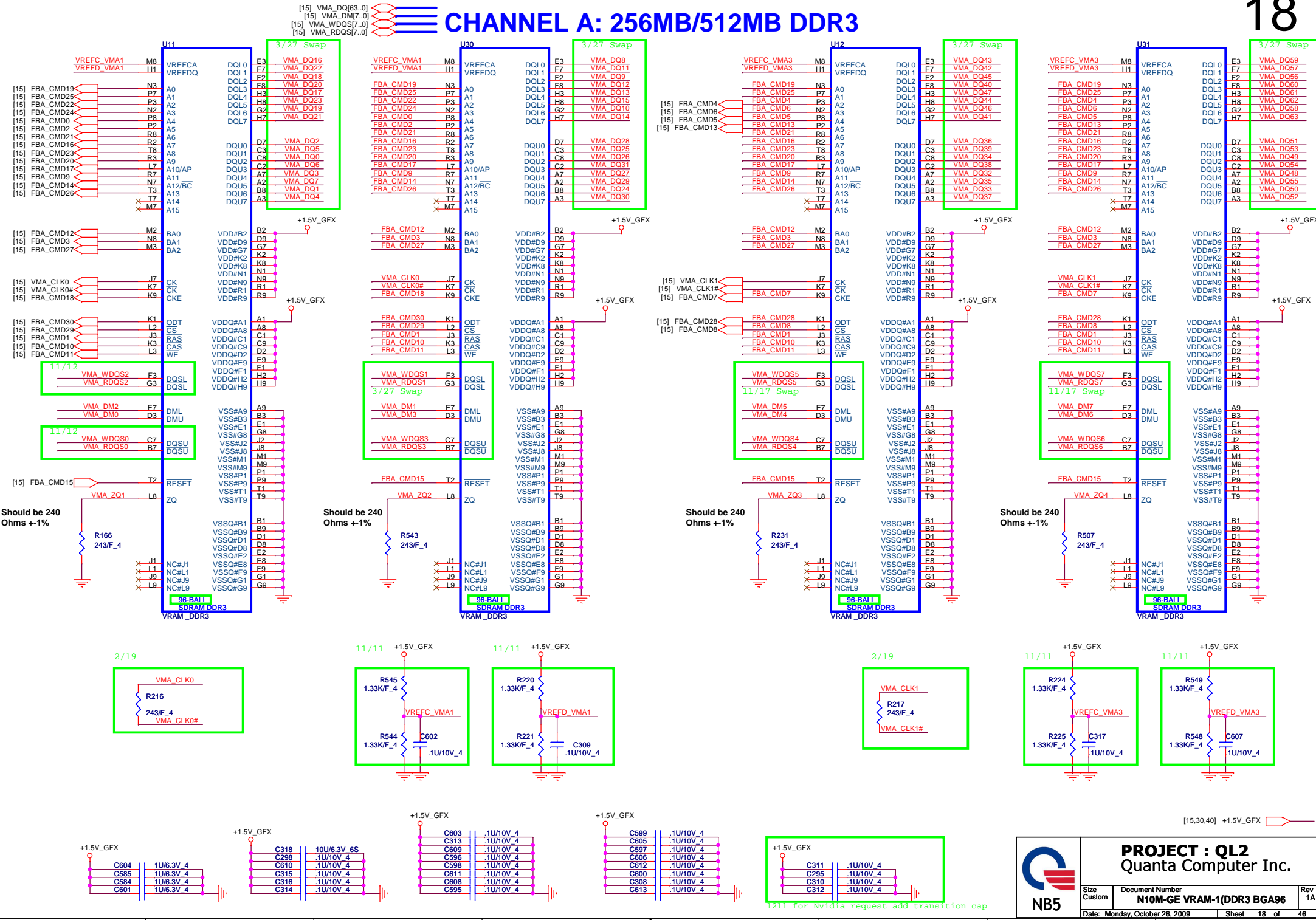
DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

SEE Datasheet for details on N10P Straps!

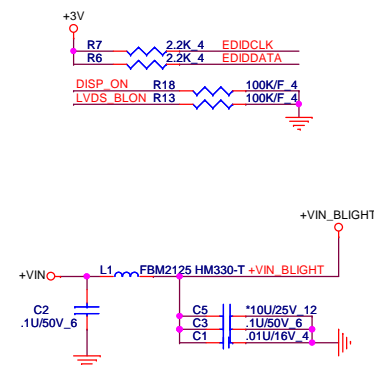
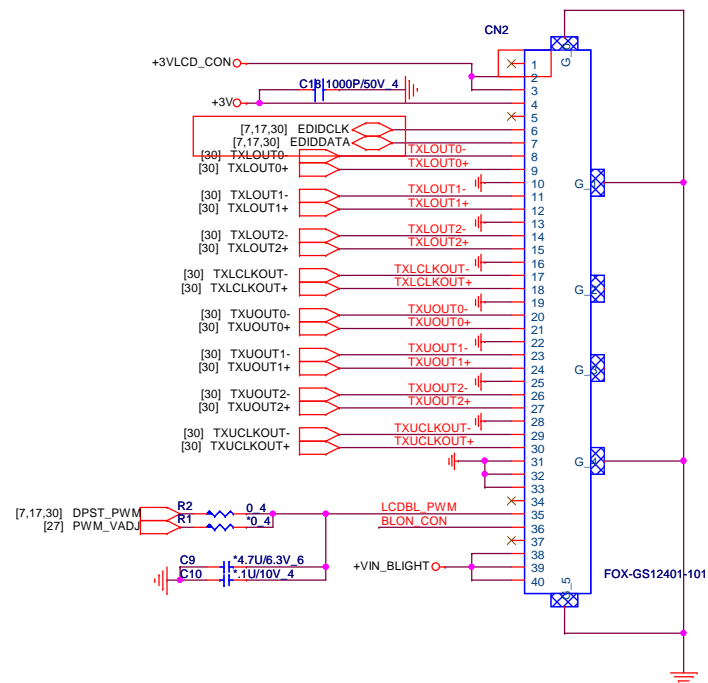
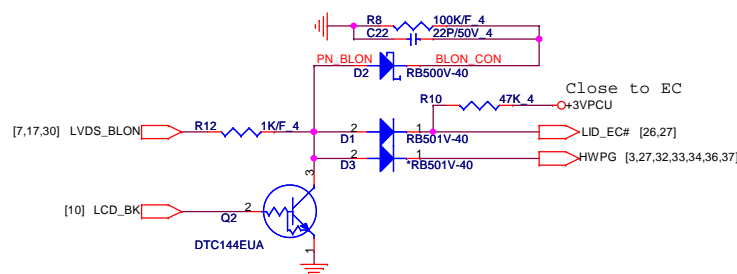
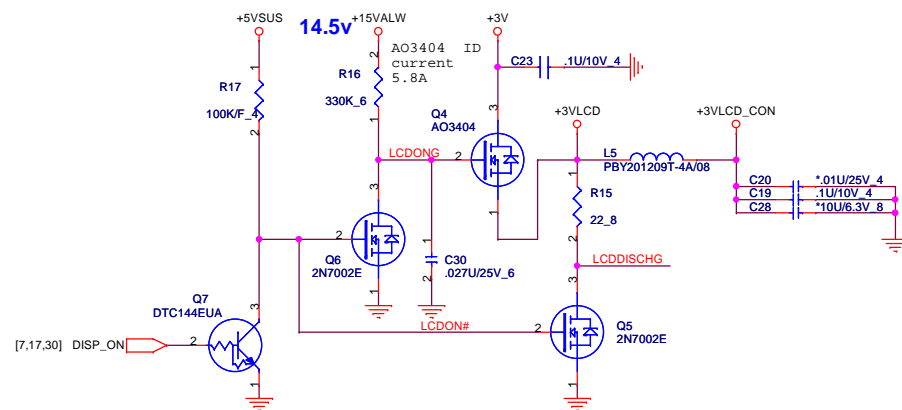
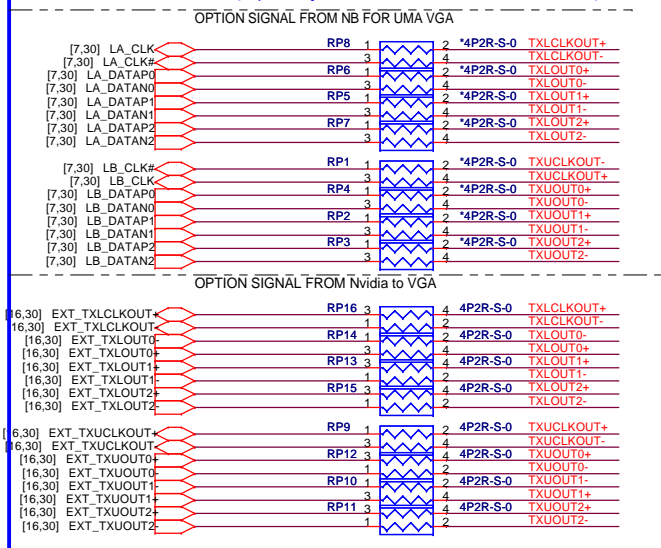
PCI_DEVID[4]/SUBVENDOR



CHANNEL A: 256MB/512MB DDR3



1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

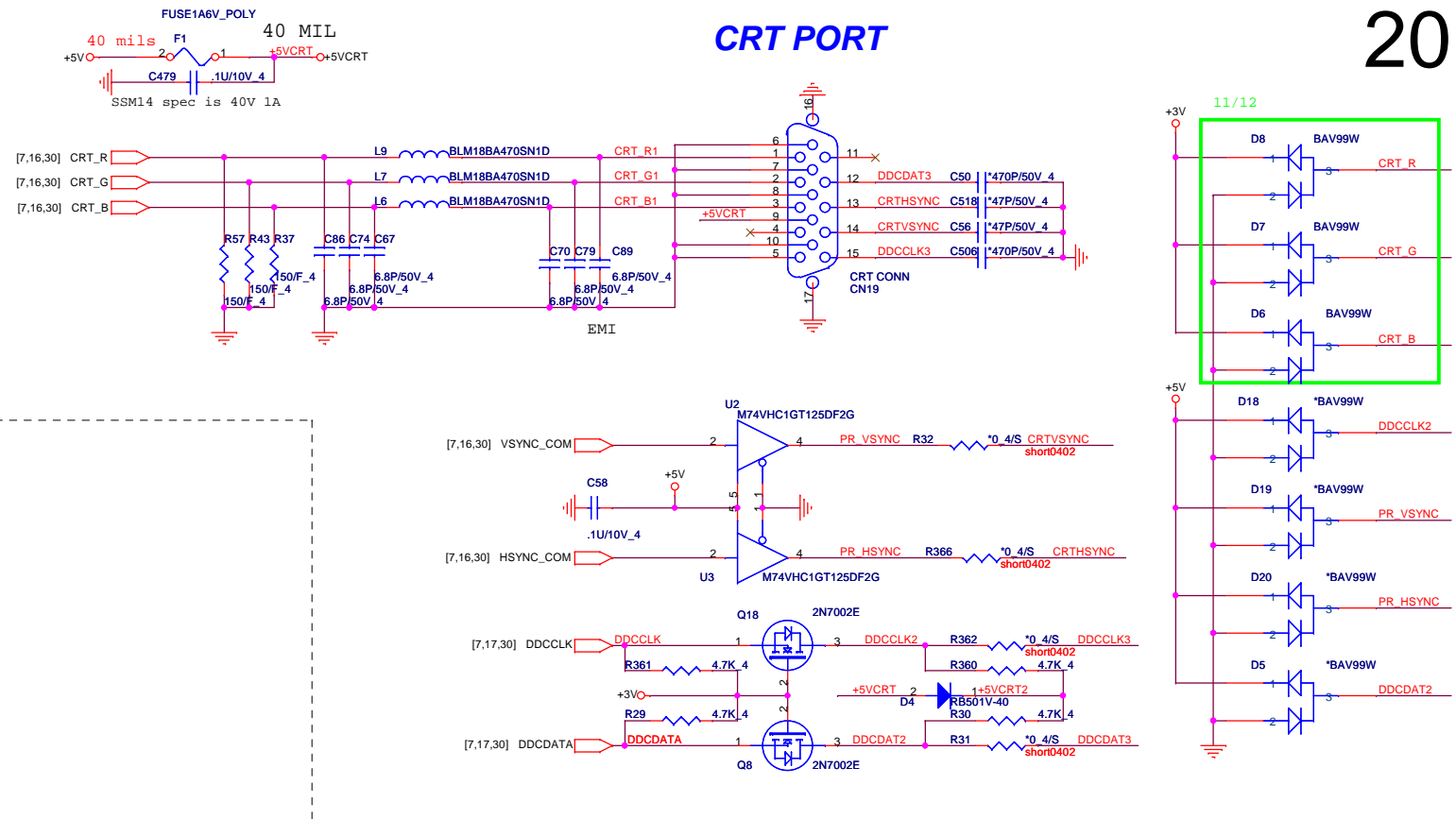


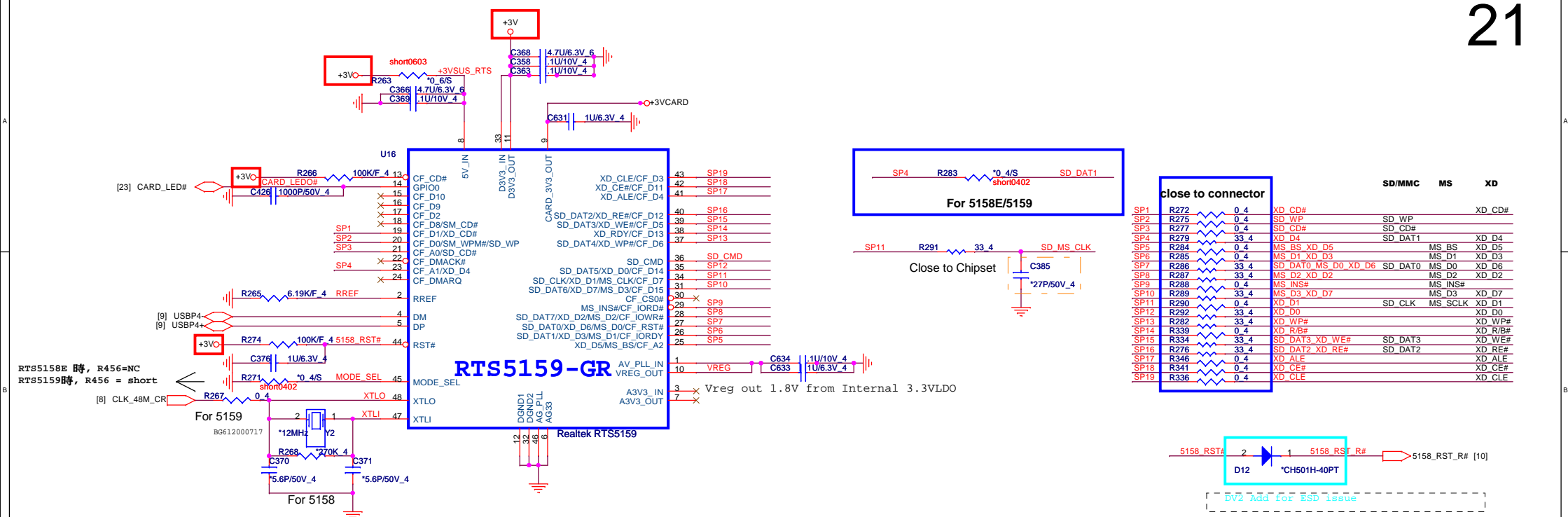
[2,3,7,8,9,10,11,12,13,20,21,22,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V
[7,23,26,27,28,32,33,34,36,38,39,40] +3VPCU
[22,25,26,38] +5VSUS
[33,38] +15VALW
[2,32,33,34,35,36,37,38,39,40] +VIN



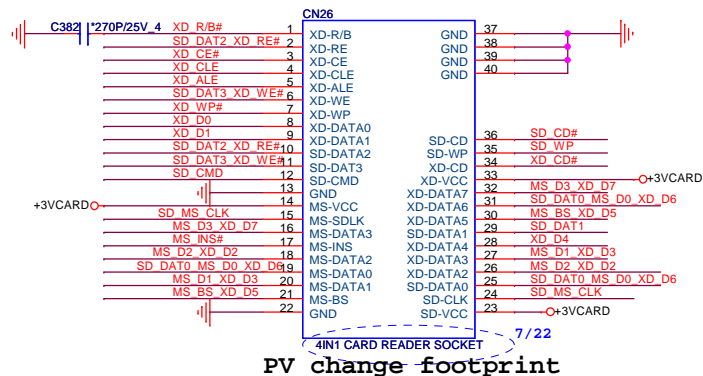
PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number LCD CONN	Rev 1A
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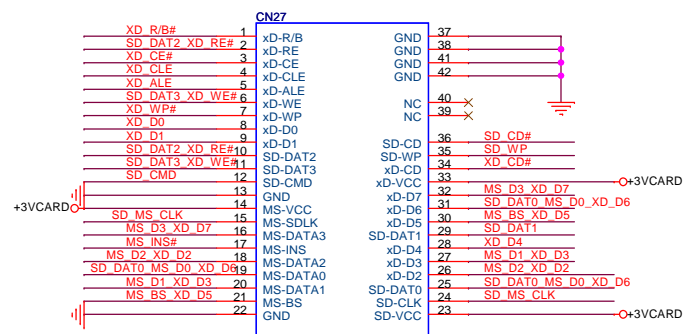


4 IN1 CARD READER XD,MMC/SD,MS/MSP

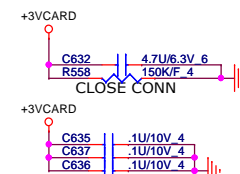


PV change footprint

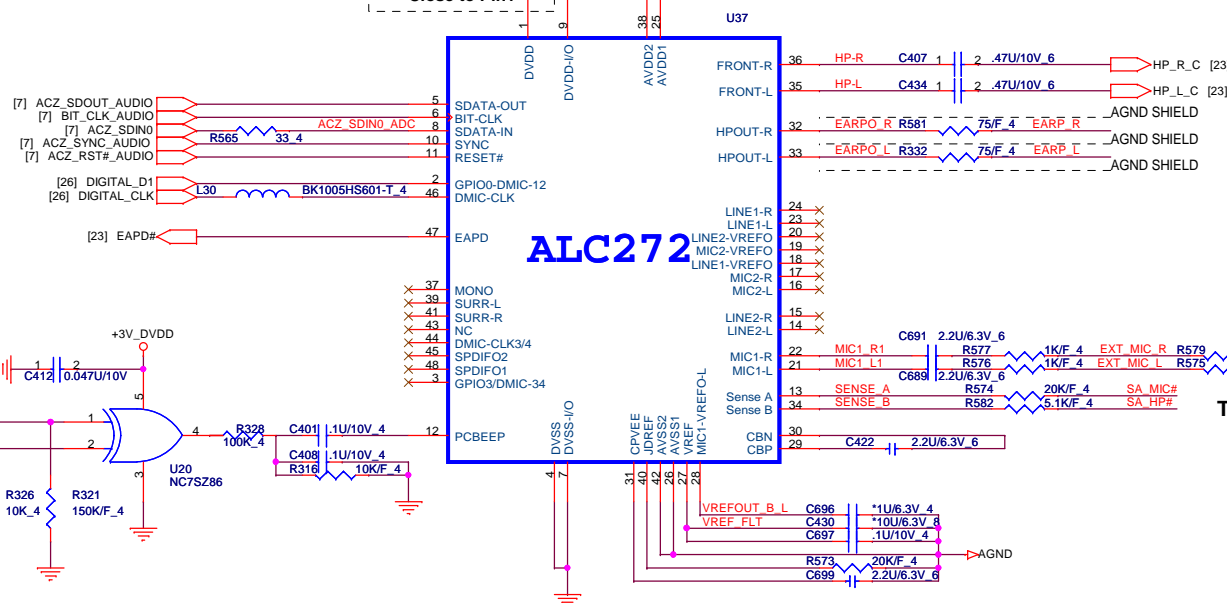
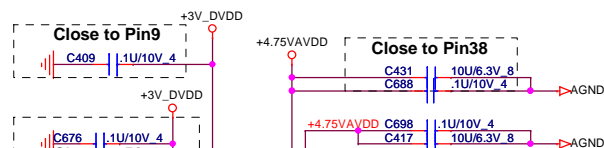
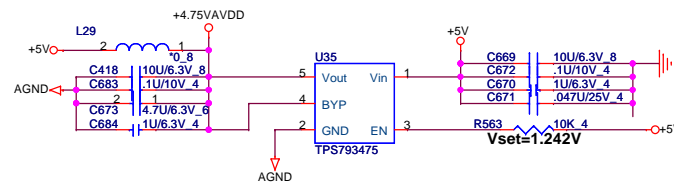
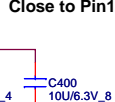
DV2 add 2'nd source



*TAI TWUM 5IN1 CARD READER SOCKET
PV change footprint

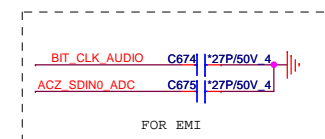


Close to Pin1



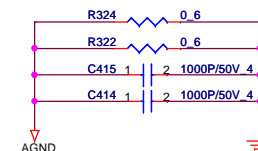
To Internal Speakers

To Headphone jack



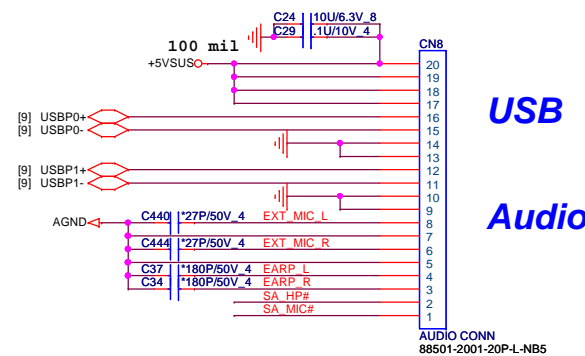
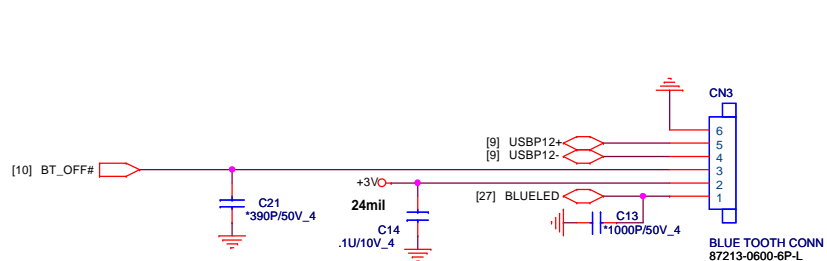
TO Audio Jack MIC

TO AUDIO/B CON.



[19,25,26,38] +5VSUS
[11,20,23,25,26,28,30,31,38] +5V
[2,3,7,8,9,10,11,12,13,19,20,21,23,24,25,26,27,28,29,30,31,32,35,38,40] +3V

Bluetooth



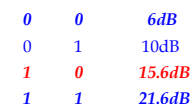
USB

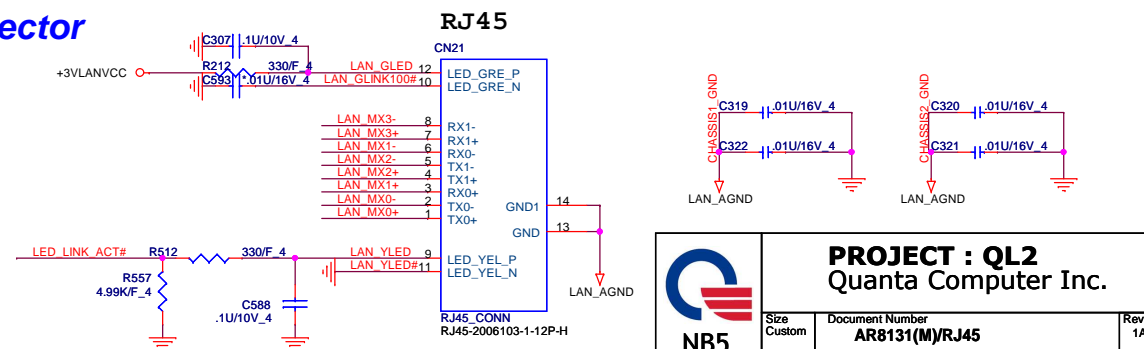
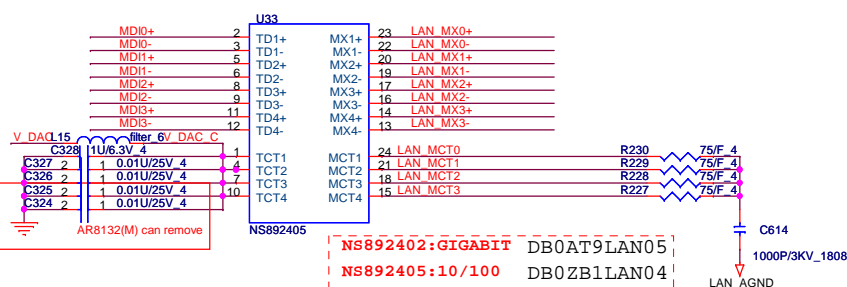
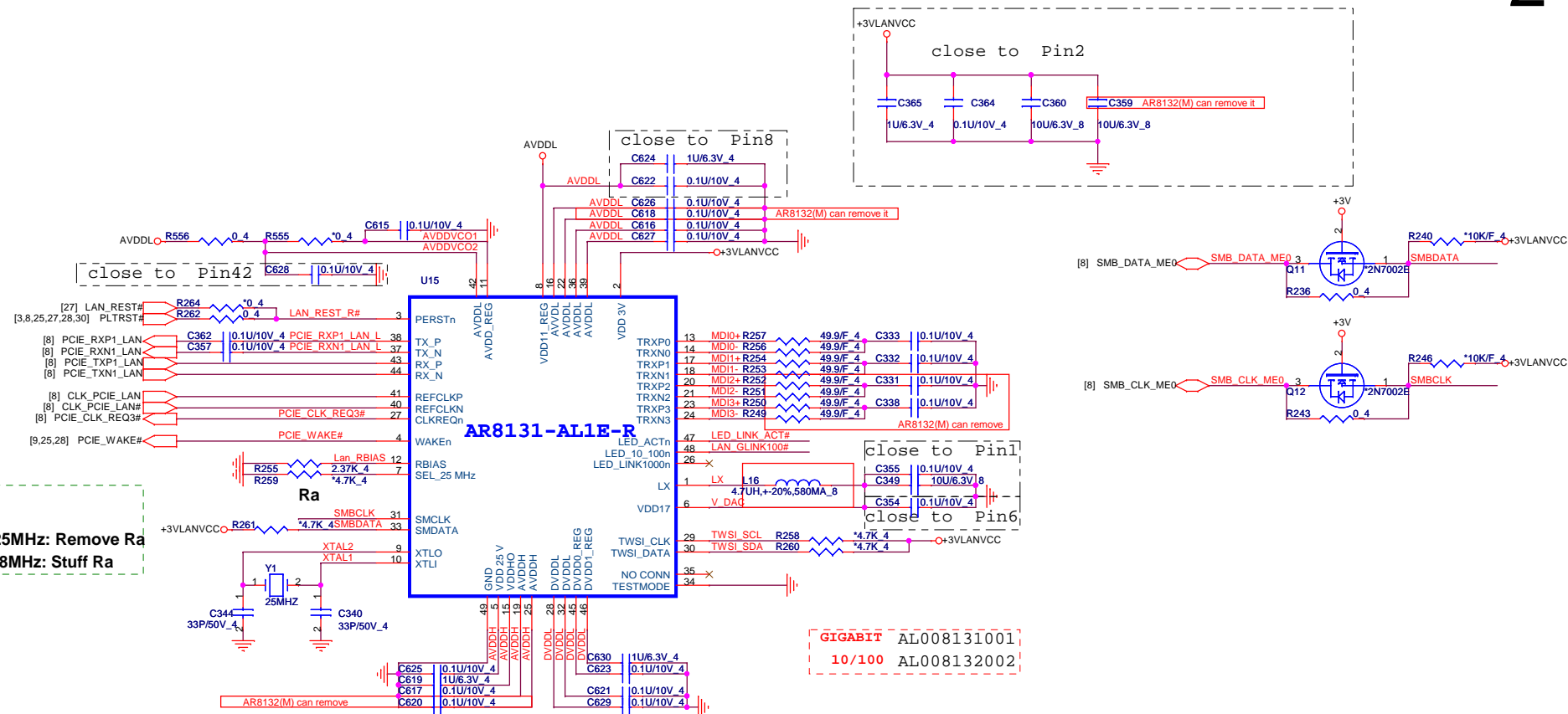
Audio



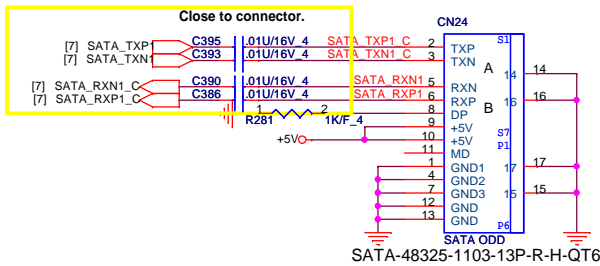
PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number Azalia ALC272/BT CONN	Rev 1A
Date: Thursday, October 29, 2009		Sheet 22 of 46

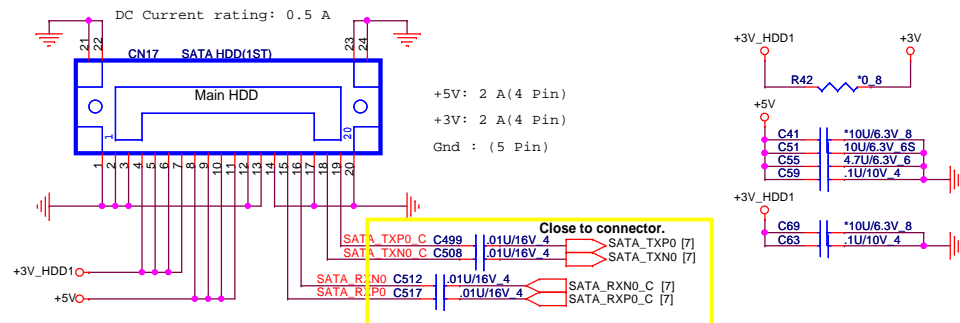




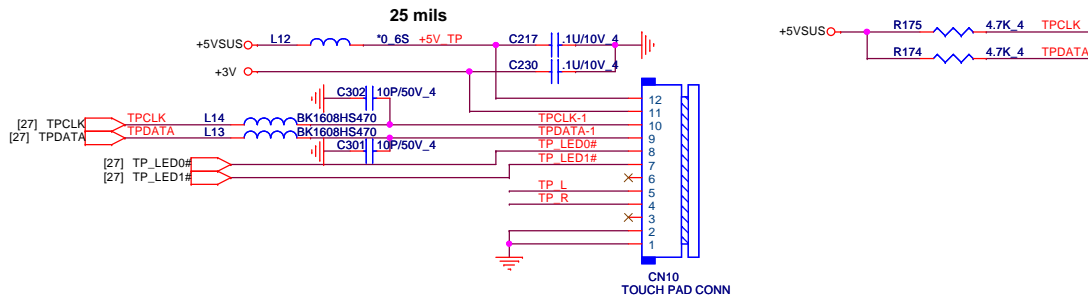
SATA ODD



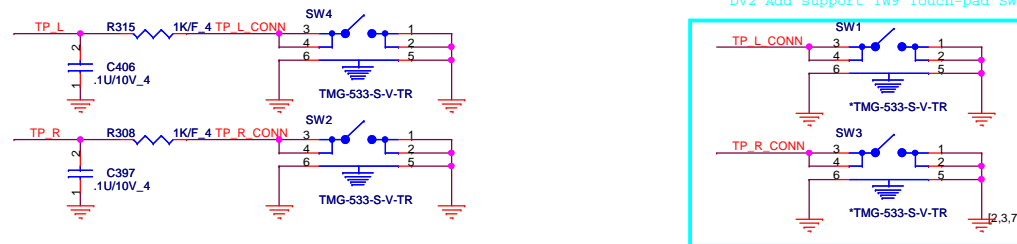
SATA_1 CONNECTOR



TOUCH PAD CONNECTOR



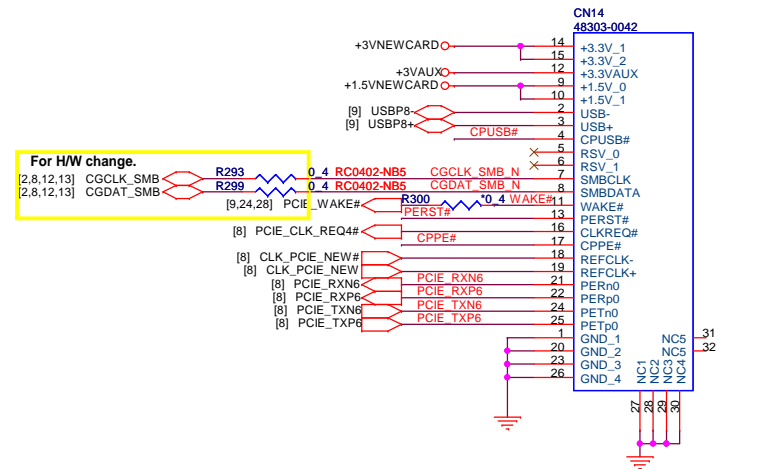
TOUCH PAD L/R SW2,SW4 in QL2 use, SW1,SW3 in SW9 use



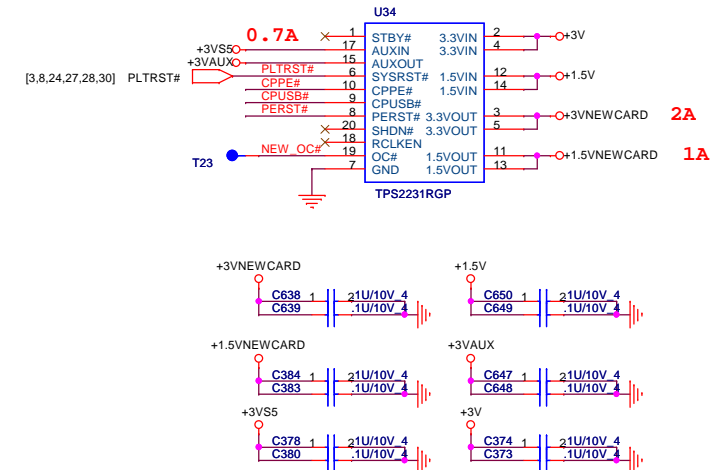
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

25



Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-1-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



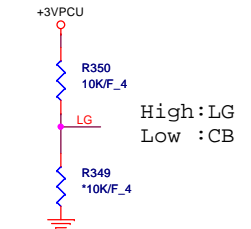
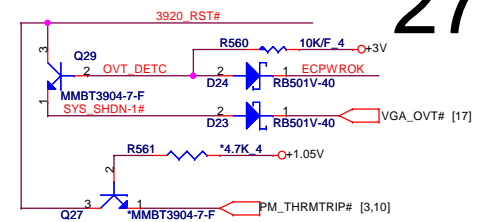
PROJECT : QL2
Quanta Computer Inc.

Size Custom Document Number ODD/HDD/NEW CARD/TP Rev 1A

Date: Thursday, October 29, 2009 Sheet 25 of 46

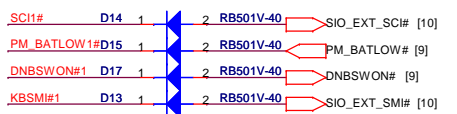
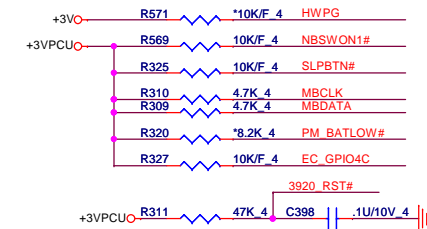
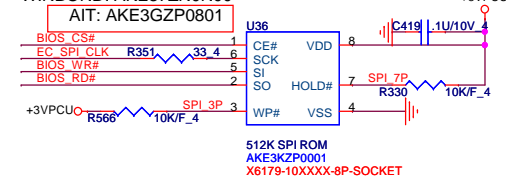
ELETRONICA

thermal shutdown circuit



SPI BIOS

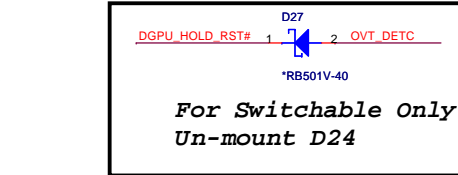
512K byte SPI ROM for EC SPI ROM Socket
 MXIC: AKE3KZP0001 DG008000031
 WINBOND: AKE37ZN0N00



PROJECT : QL2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

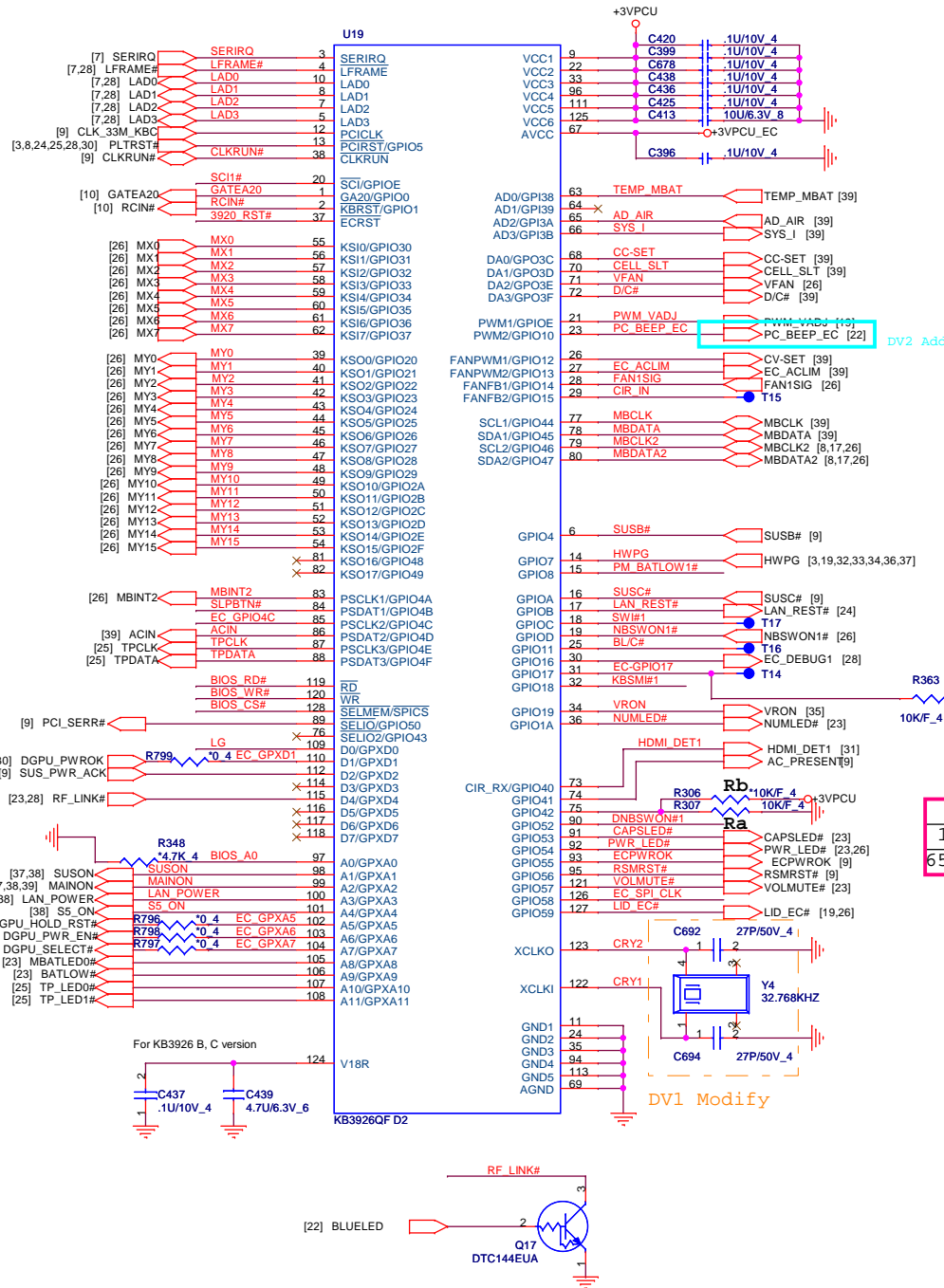
Date: Wednesday, October 28, 2009 Sheet: 27 of 46



*For Switchable Only
 Un-mount D24*

Adapter table select

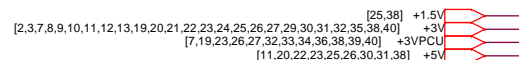
ID	Ra	Rb
120W	10K	N/A
65W/90W	N/A	10K



[9.30] EDID_SELECT# → R800 → 0.4 EC GPXA7

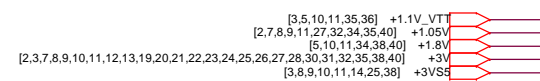
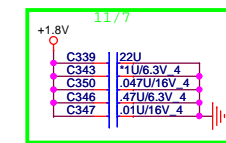
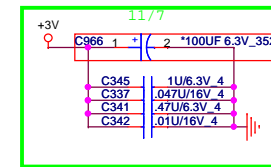
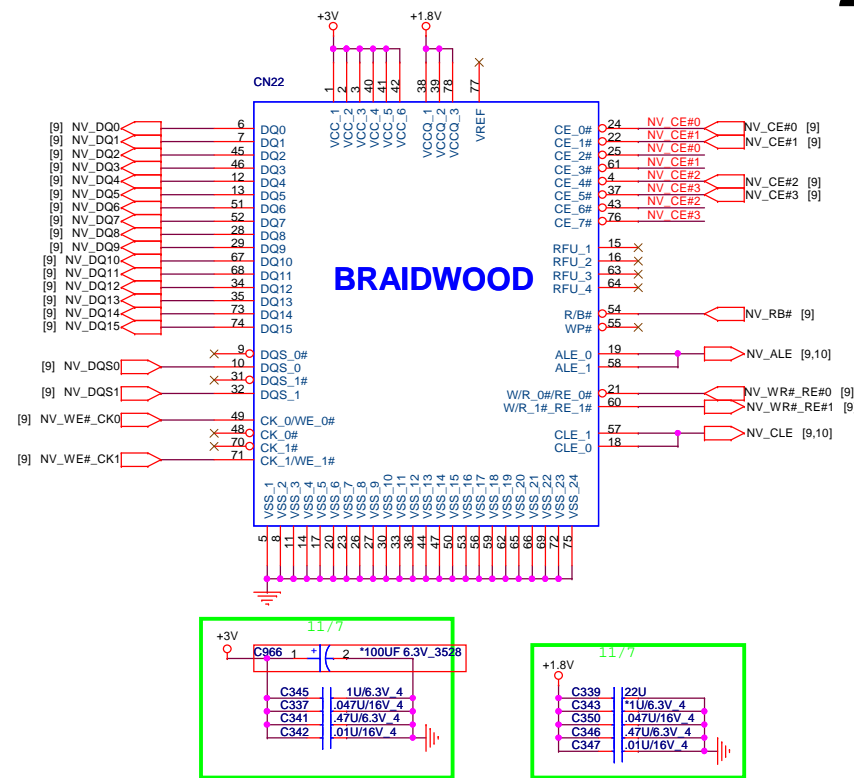
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,28,29,30,31,32,35,38,40] +3V
 [7,19,23,26,28,32,33,34,36,38,39,40] +3VPCU
 [32,33,34,35,36,37,38] +5VPCU

28

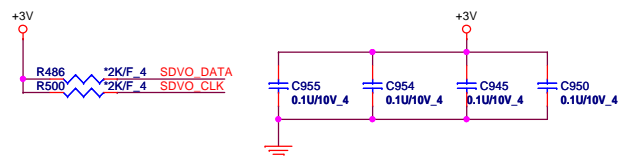
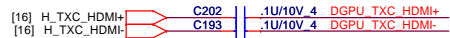
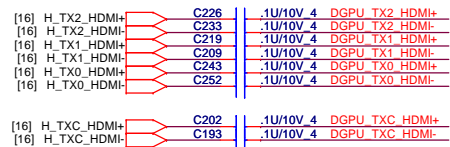


PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN X2	Rev 1A
Date: Thursday, October 29, 2009		Sheet 28 of 46



DGPU HDMI



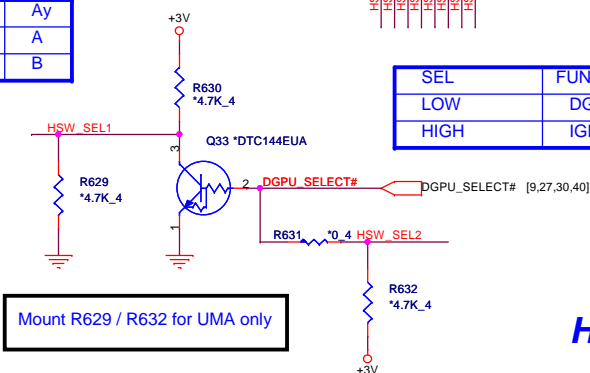
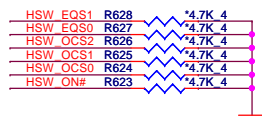
OC SETTING

S2	S1	S0 = 1 : 1 : 1	500mV	0dB	Default
S2	S1	S0 = 1 : 1 : 0	750mV	0dB	
S2	S1	S0 = 1 : 0 : 1	1000mV	0dB	
S2	S1	S0 = 1 : 0 : 0	600mV	0dB	
S2	S1	S0 = 0 : 1 : 1	500mV	0dB	
S2	S1	S0 = 0 : 1 : 0	500mV	1.5dB	
S2	S1	S0 = 0 : 0 : 1	500mV	3.5dB	
S2	S1	S0 = 0 : 0 : 0	500mV	6dB	

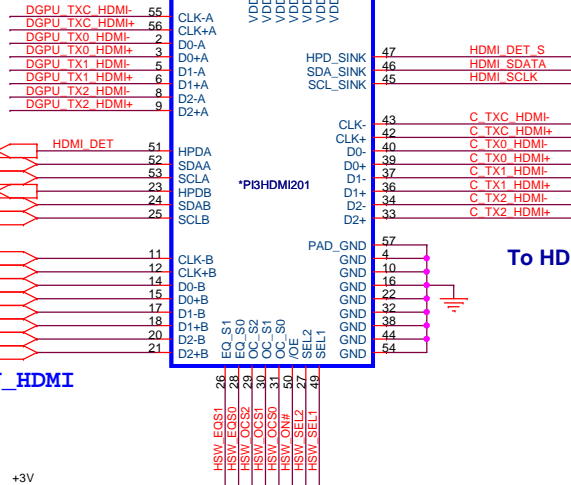
OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B

EQ SETTING

S1 S0 = 1 : 1 3dB Default
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB



Mount R629 / R632 for UMA only

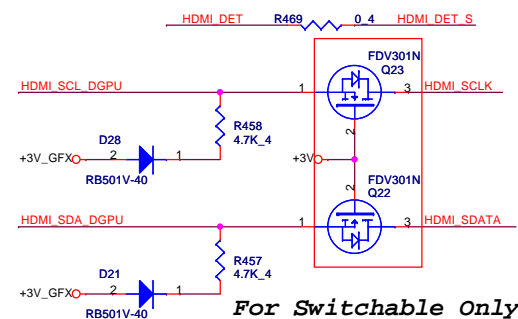
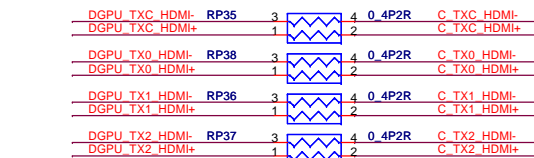
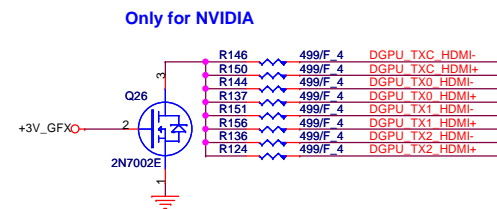
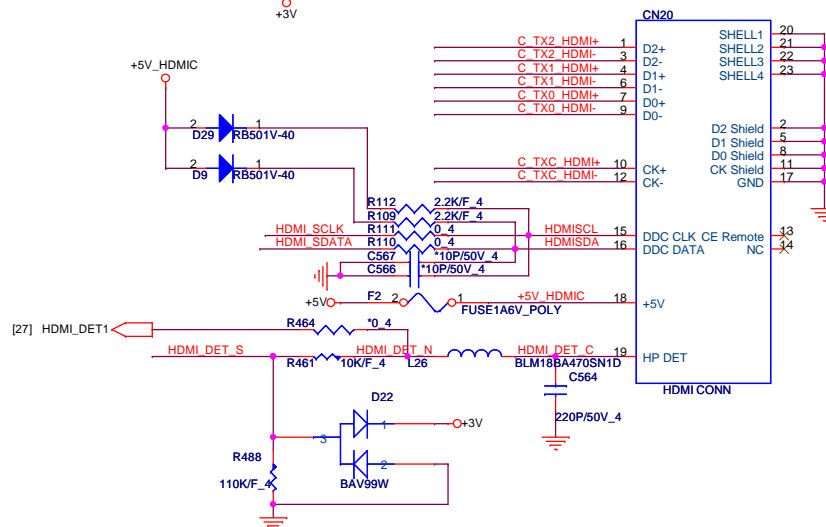


HDMI Switch

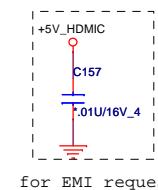
To HDMI Conn.

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

HDMI PORT



For Switchable Only



for EMI request

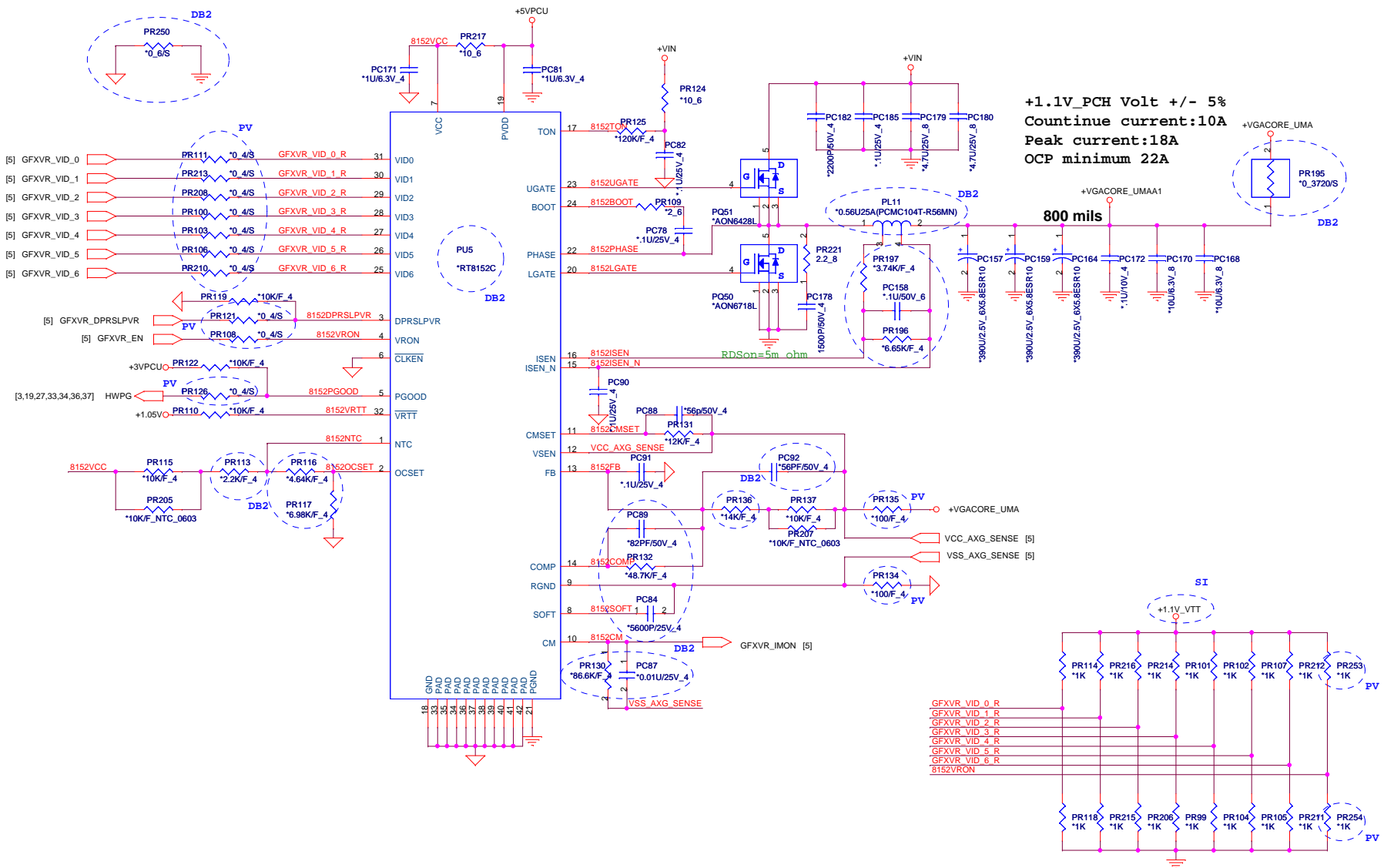


PROJECT : QL2
Quanta Computer Inc.

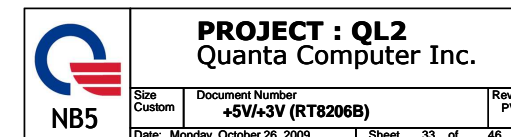
Size	A3
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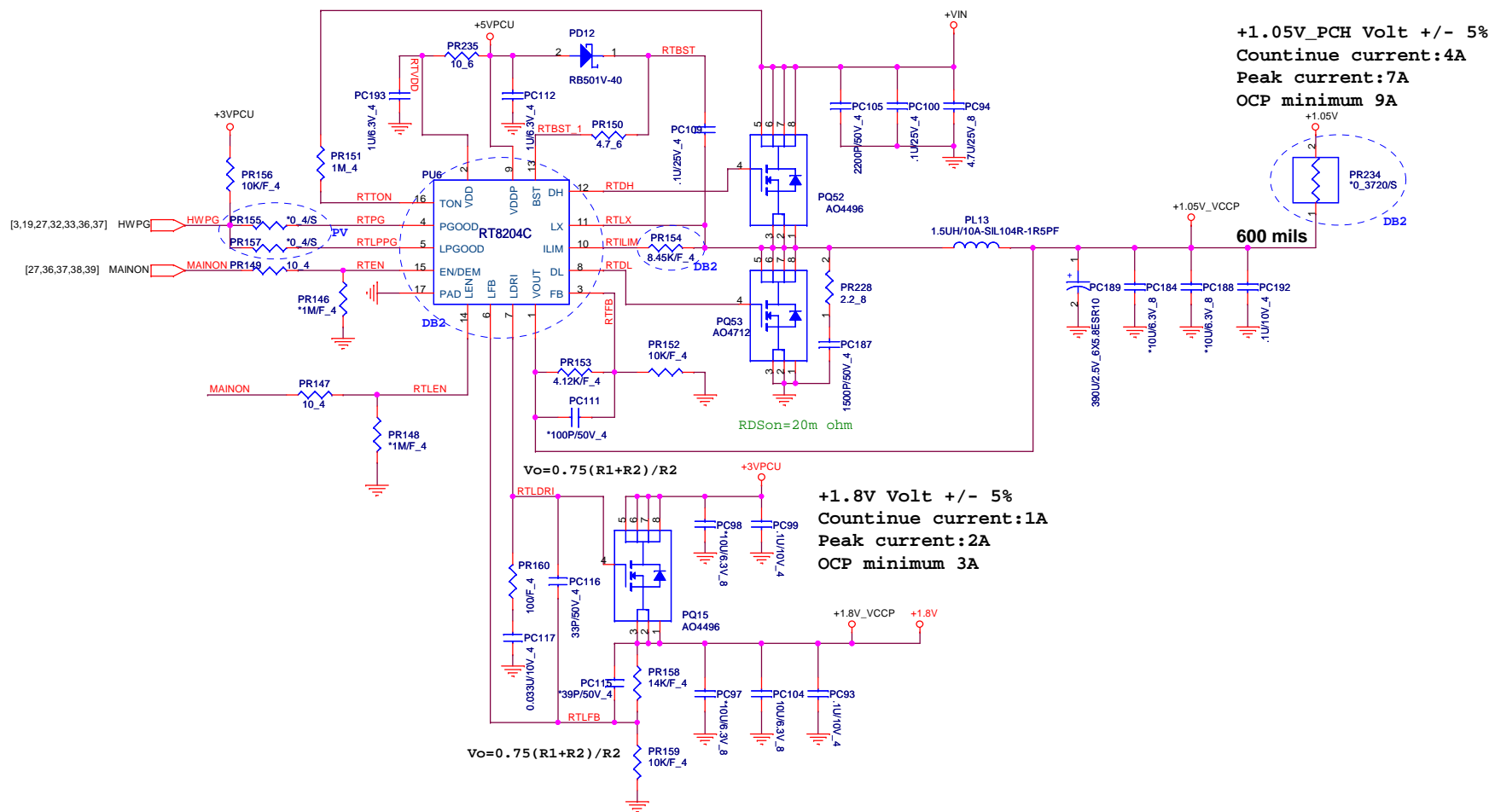
Document Number	HDMI Switch
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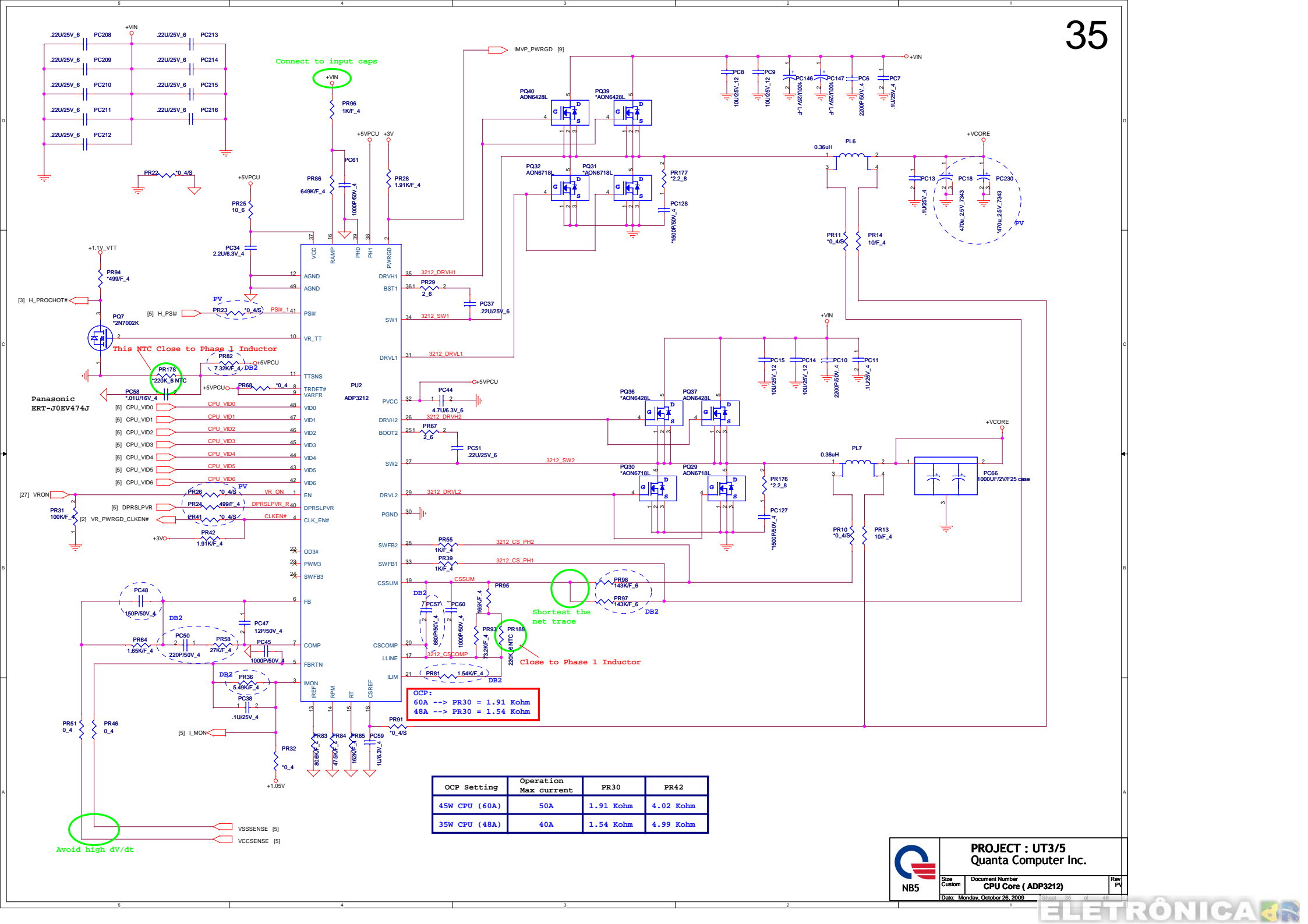
Rev
1A



+1.1V_PCH Volt +/- 5%
Countinue current:10A
Peak current:18A
OCp minimum 22A



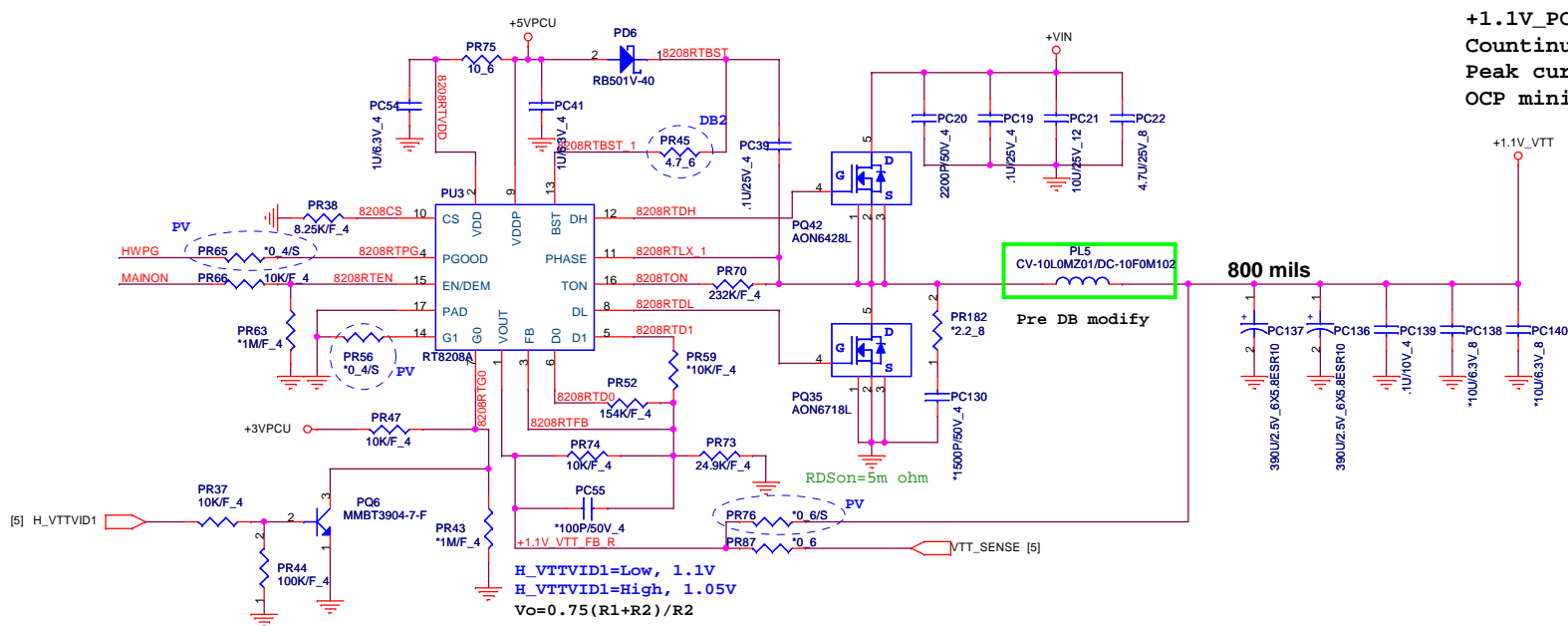
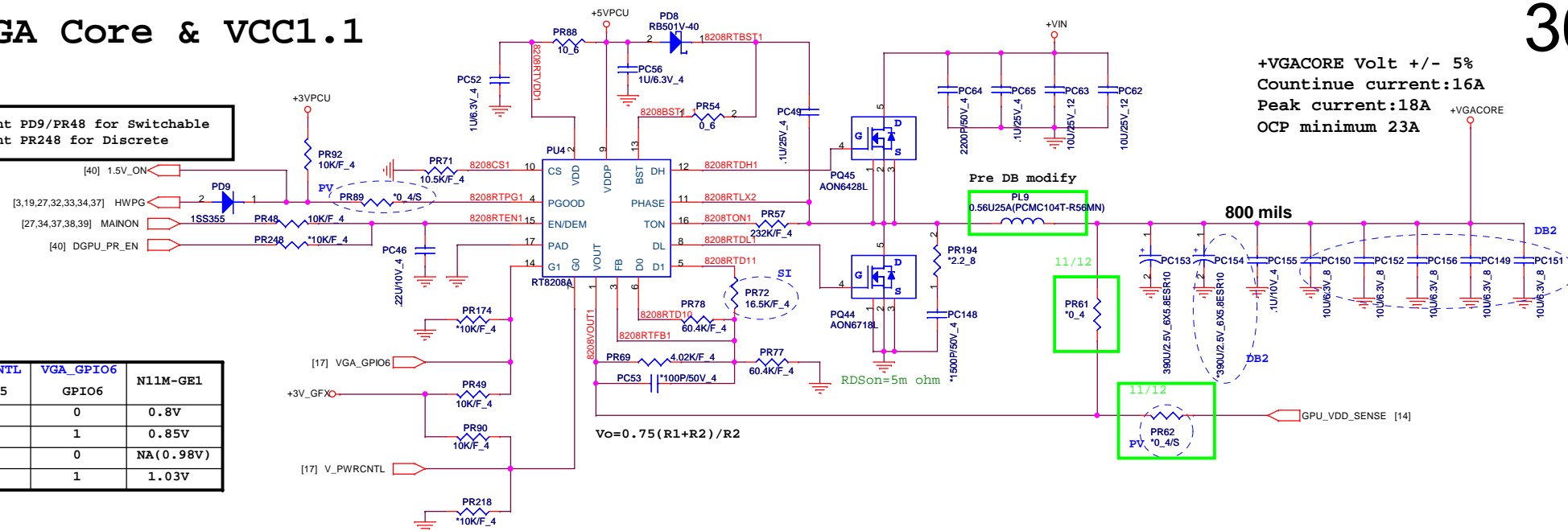
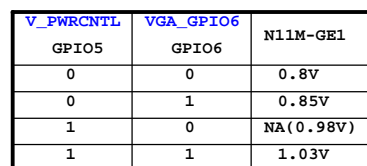




OCP Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm

36

+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:18A
OCP minimum 23A

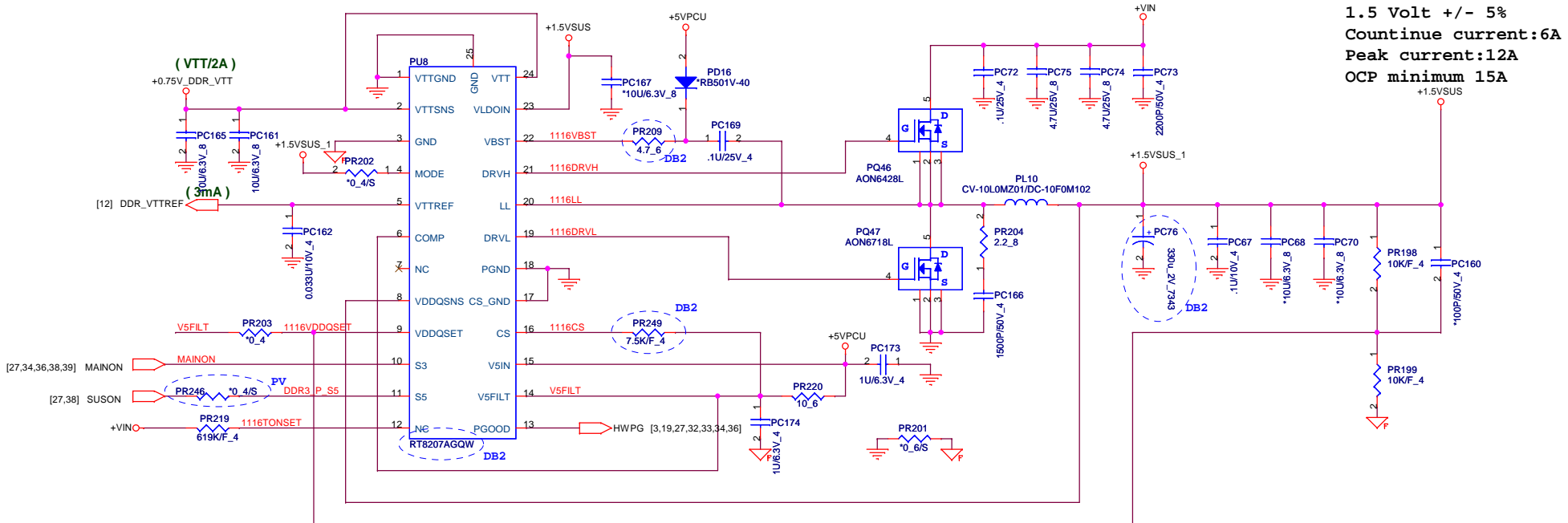


```
+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A
```



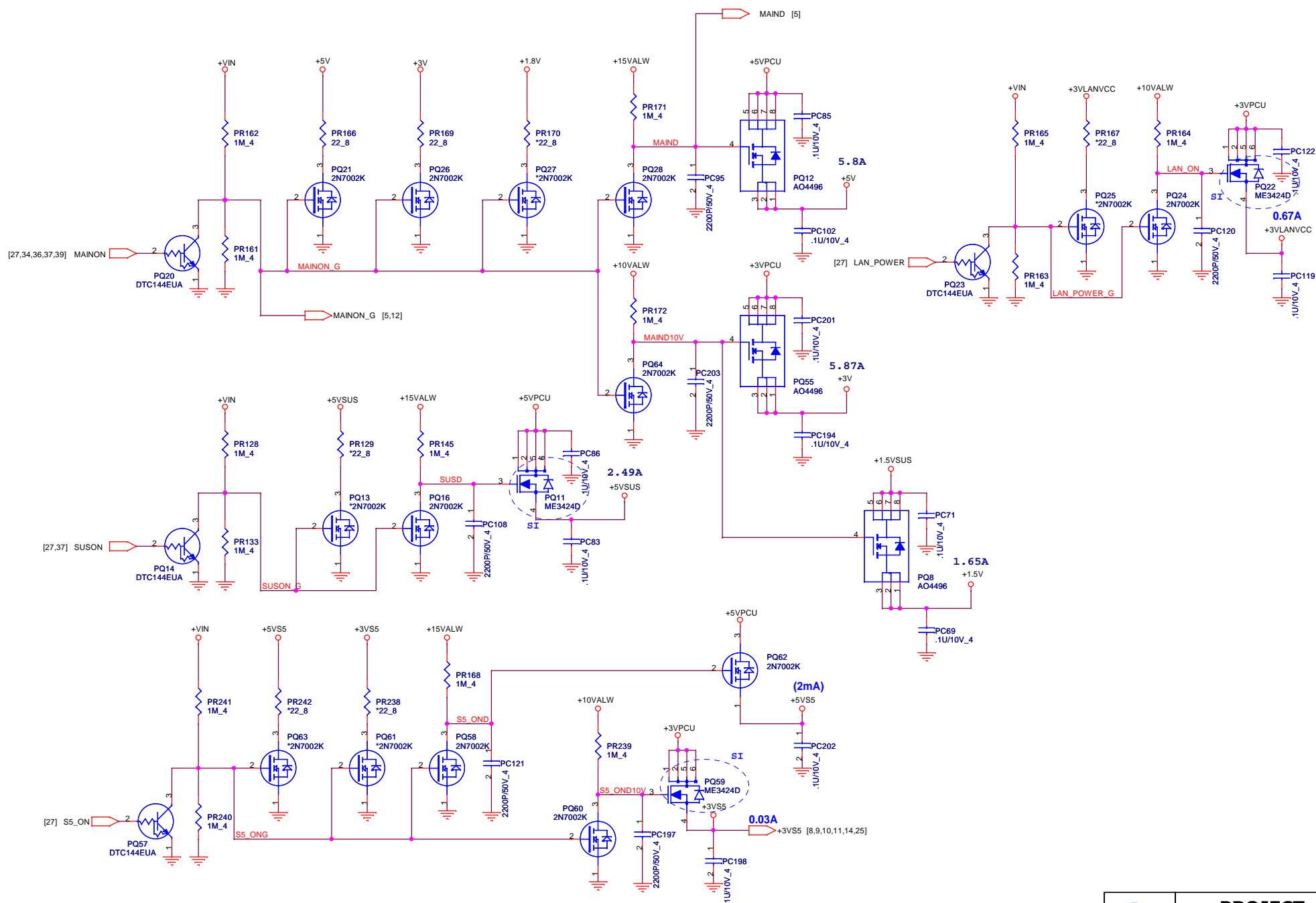
PROJECT : QL2
Quanta Computer Inc.

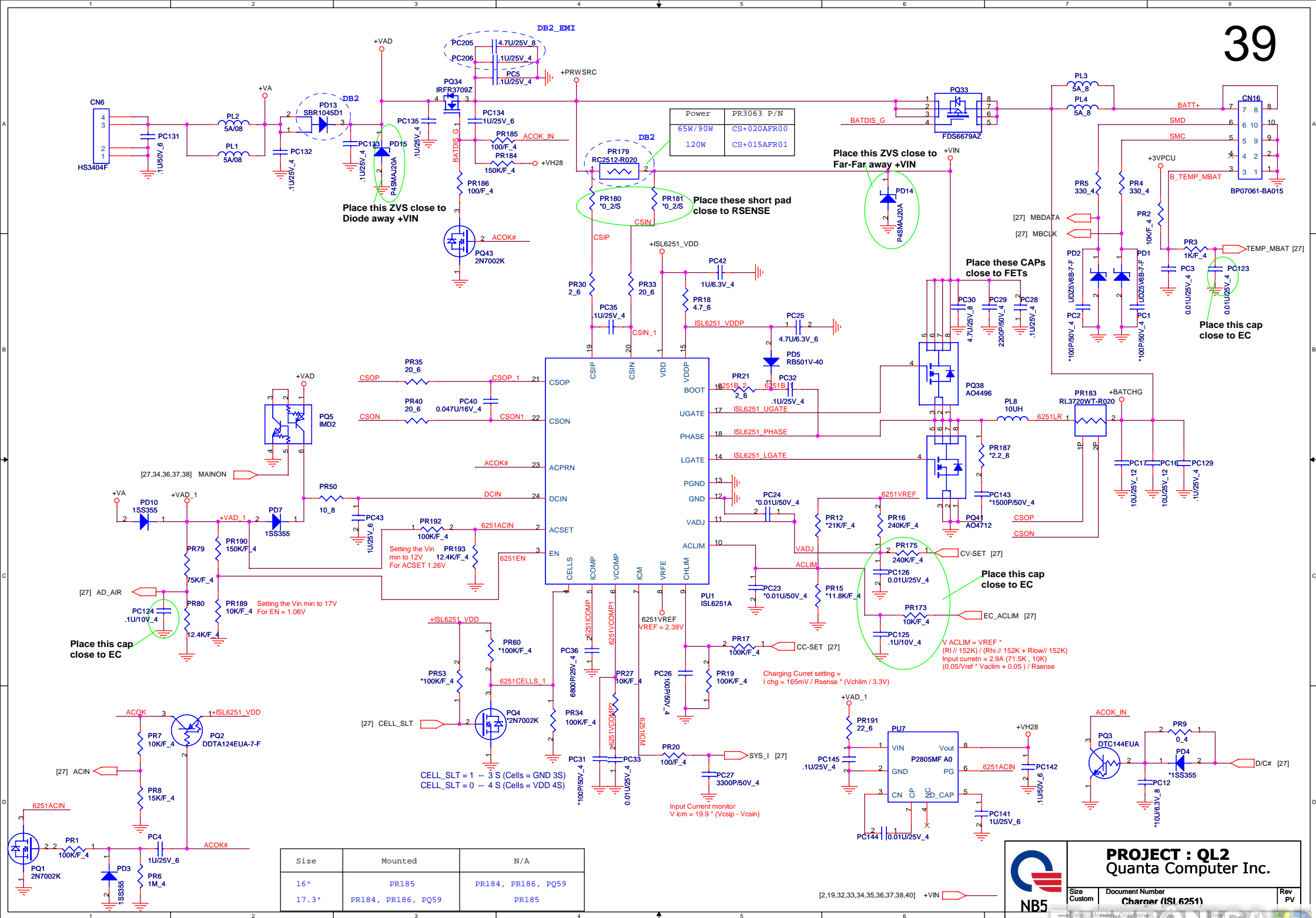
Size Custom	Document Number +1.1V_VTT/VGA Core RT820A	Re I
Date: Monday, October 26, 2009		Sheet 36 of 46



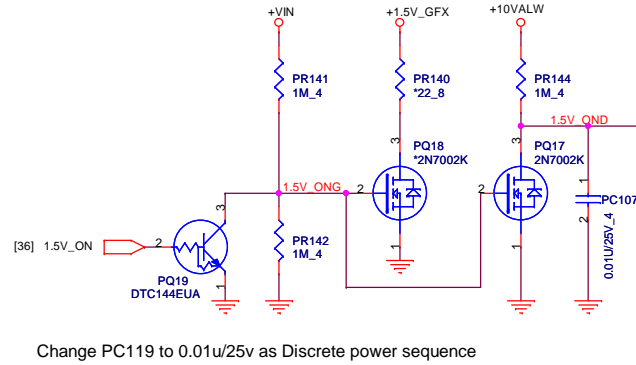
PROJECT : QL2
Quanta Computer Inc.

Size Custom	Document Number DDR3 (RT8207)	Rev PV
Date: Thursday, October 29, 2009	Sheet 37 of 46	



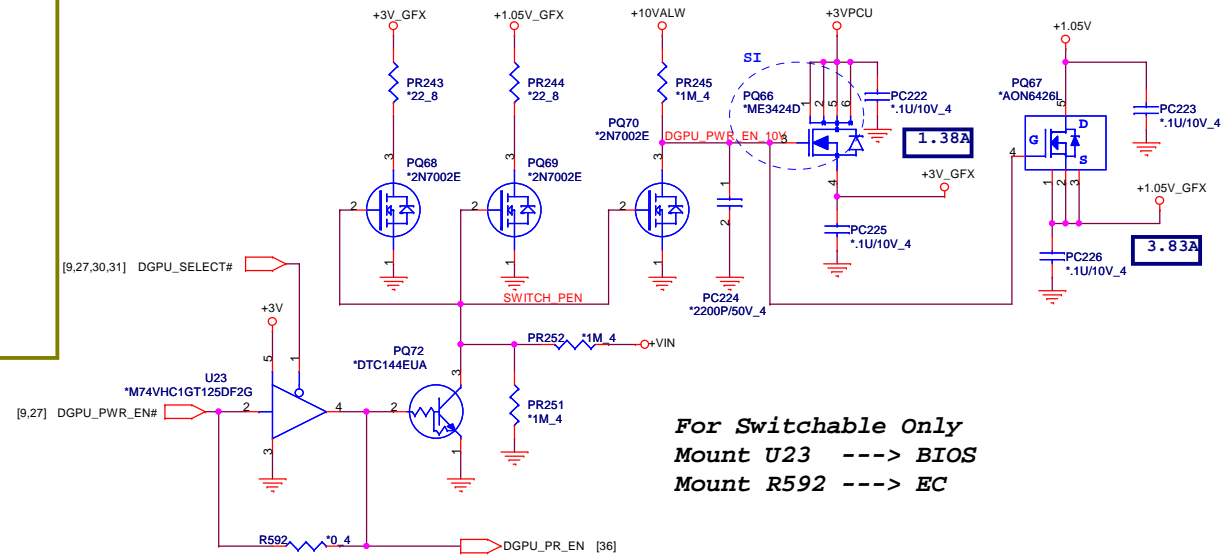
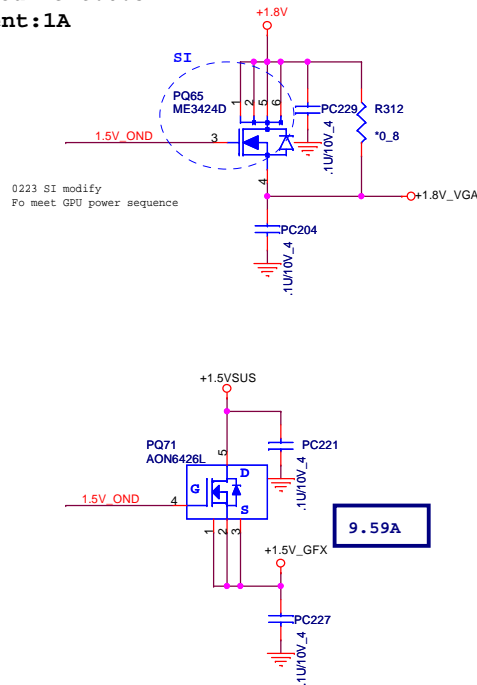


For Discrete or switchable Only



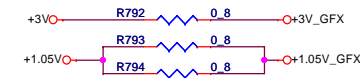
For Discrete or switchable Only

+1.8 Volt +/- 0.1V
 Countinue current:0.3A
 Peak current:1A



For Switchable Only
 Mount U23 ---> BIOS
 Mount R592 ---> EC

For Discrete Only

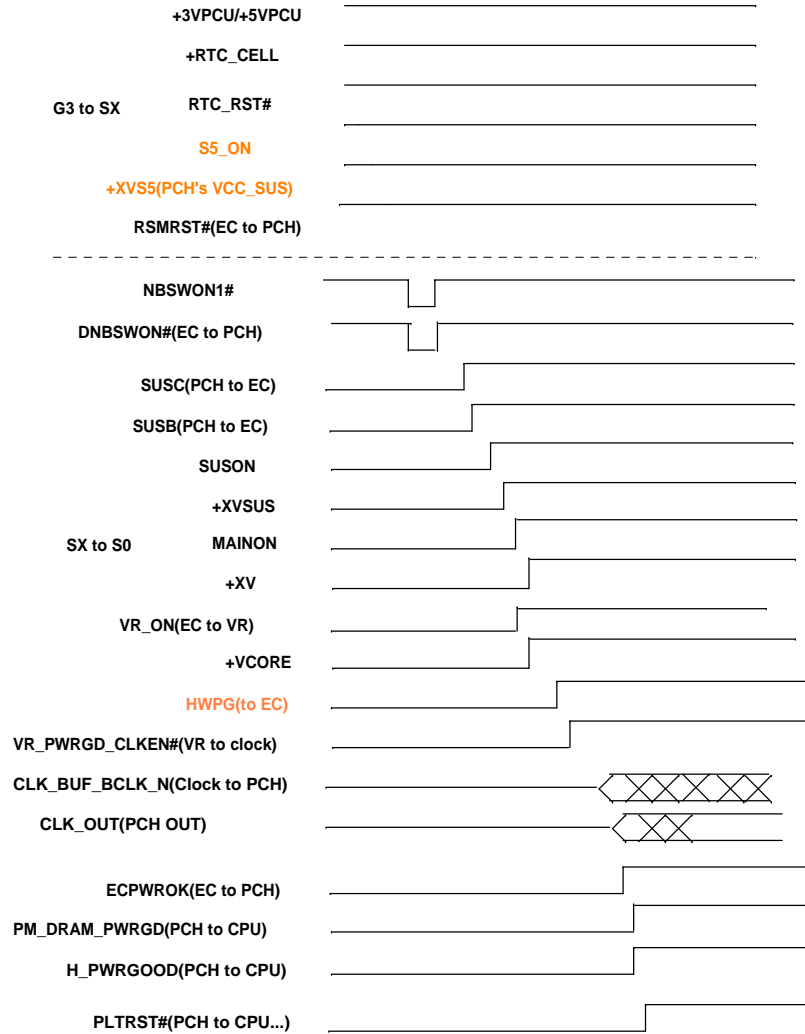


For Hybrid DGPU Power Rails Sequence

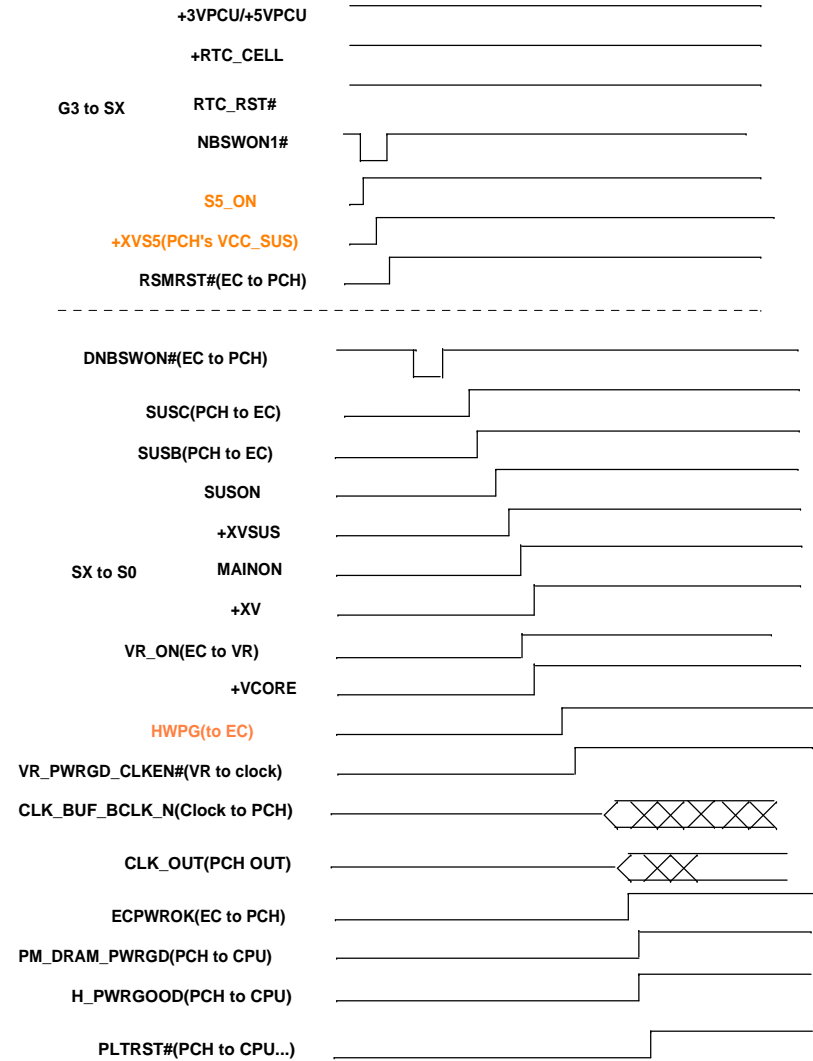
1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

Power up sequence

LAN/RTC WAKE UP ENABLE.



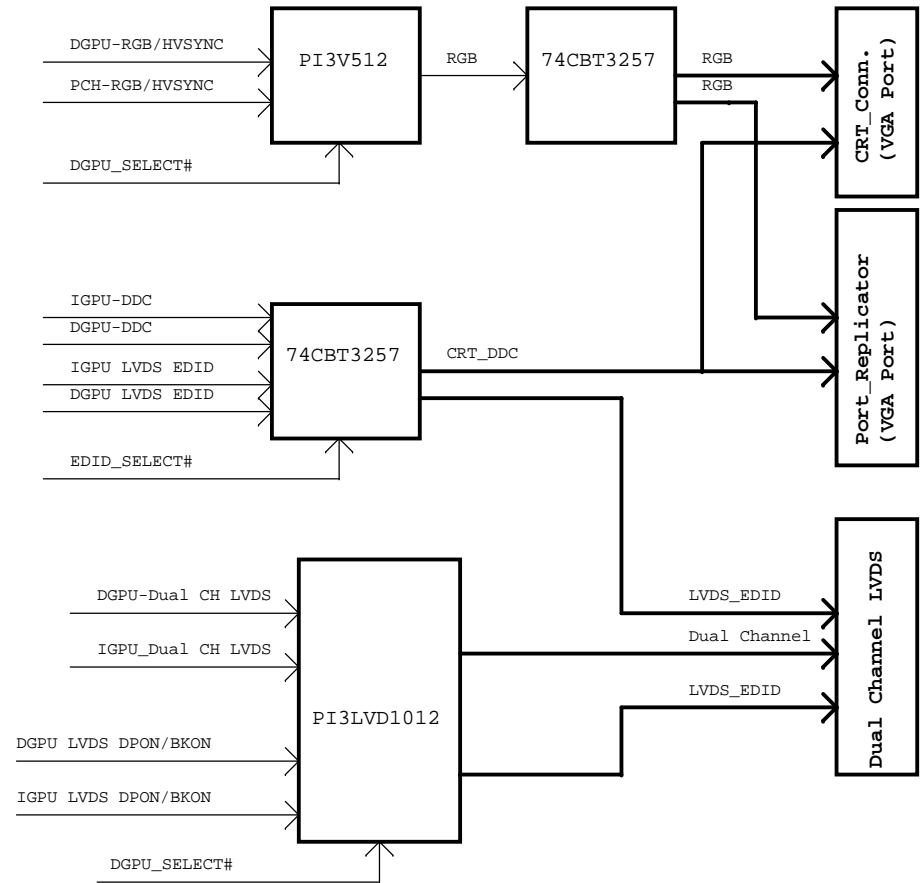
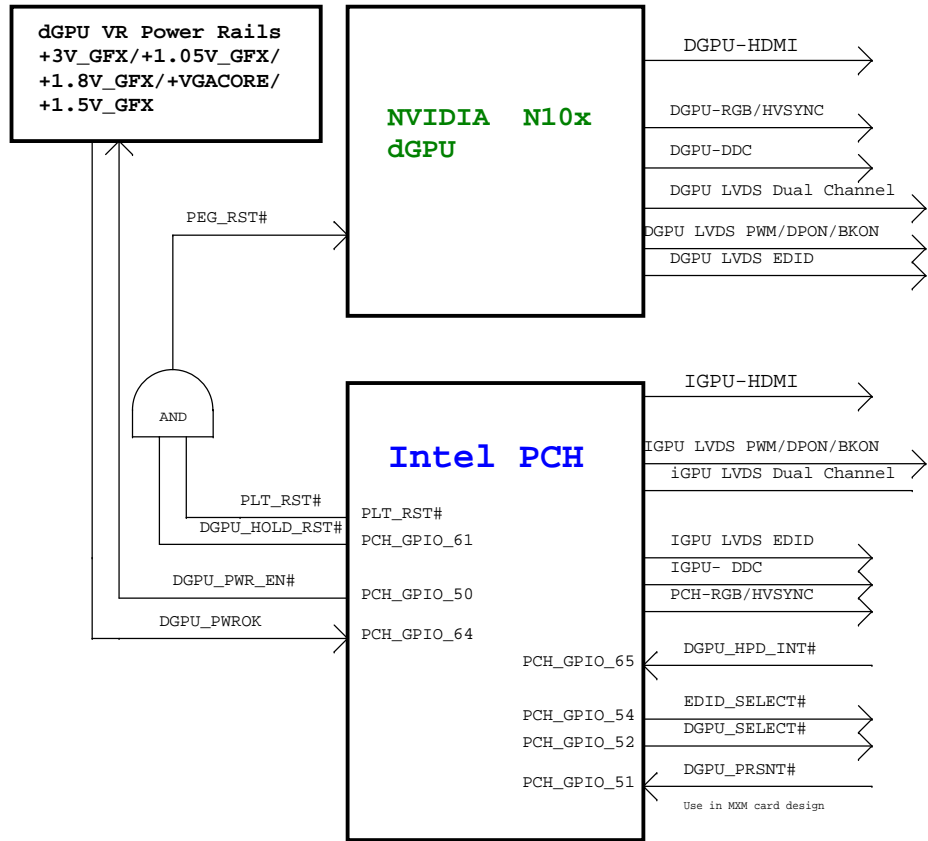
LAN/RTC WAKE UP DISABLE.



PROJECT : QL2
Quanta Computer Inc.

Size Custom Document Number
Power up sequence Rev 1A

Date: Monday, October 26, 2009 Sheet 41 of 46



Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSENT#
PCH_GPIO53	PWM_SELECT#

